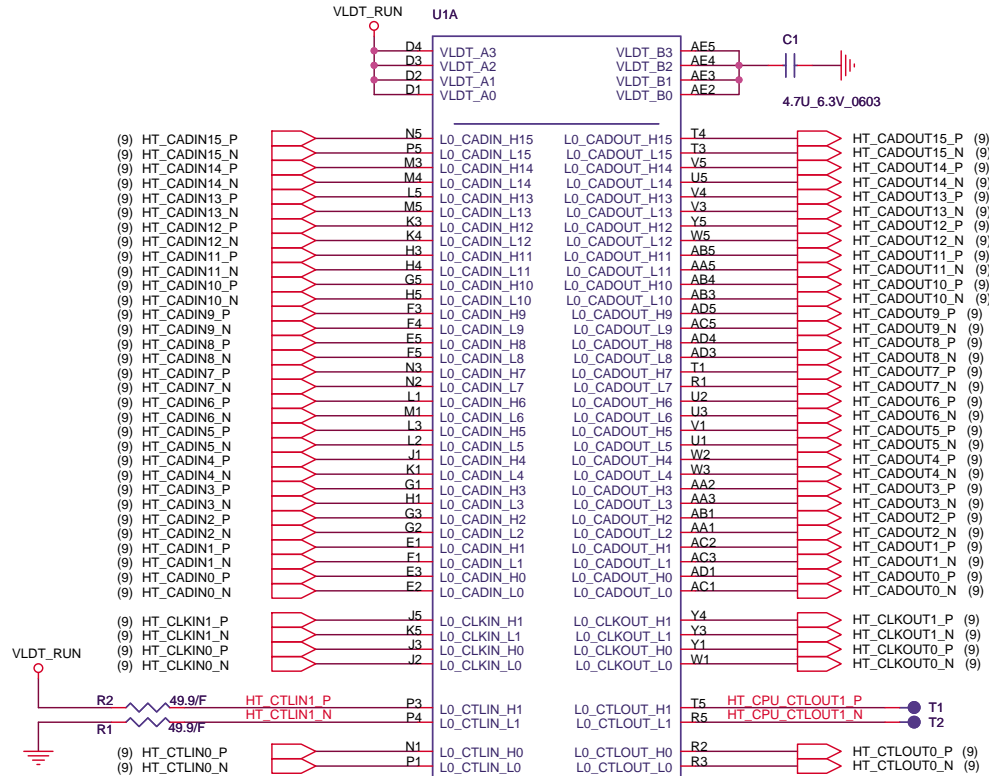


# INDEX

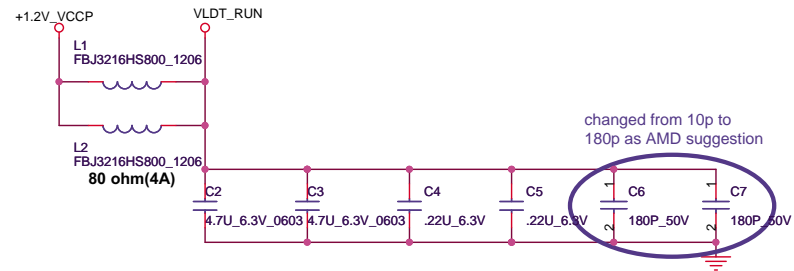
Page	Description
1	BLOCK DIAGRAM
2	FRONT PAGE
3	ATHLON64 HT I/F
4	ATHLON64 DDRII MEMORY
5	ATHLON64 CTRL & DEBUG
6	ATHLON64 PWR & GND
7	DDRII SODIMMX2
8	DDRII TERMINATION
9	RS485-HT LINK0 I/F
10	RS485-PCIE LINK I/F
11	RS485-LVDS
12	RS485-POWER
13	CLOCK GENERATOR
14	SB600M-PCIE/PCI/LPC
15	SB600M ACPI/USB/AC97
16	SB600M HDD/POWER
17	SB600M STRAPS
18	LCD CONN
19	CRT
20	5C832/PCI
21	CARD READER
22	CARD READER CONN
23	SATA HDD & PATA ODD
24	MINI Card
25	MINI Card
26	MDC CONN
27	PC97551 & FLASH
28	USB
29	EMI & Screw hole
30	SWITCH & TP & LED
31	Azelia CODEC
32	AUDIO CONN
33	LAN(BCM4401)
34	LAN JACK
35	KB & THERMAL & FAN
36	CHARGER (MAX8731)
37	VHCORE (MAX8774)
38	SYSTEM (MAX8734)
39	VCCP & DDR2 (MAX8743)
40	RUN POWER SW
41	DCIN,Batt
42	MINI PCI(for debug)
43	Power On Sequence
44	Power On Diagram
45	SMBUS BLOCK

**PROCESSOR HYPERTRANSPORT INTERFACE**

VLDT\_Ax AND VLDT\_Bx ARE CONNECTED TO THE LDT\_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1  
Processor Socket

**LAYOUT: Place bypass cap on topside of board**

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS  
PLACE CLOSE TO VLDT0 POWER PINS



QUANTA  
COMPUTER

Title  
ATHLON64 HT I/F

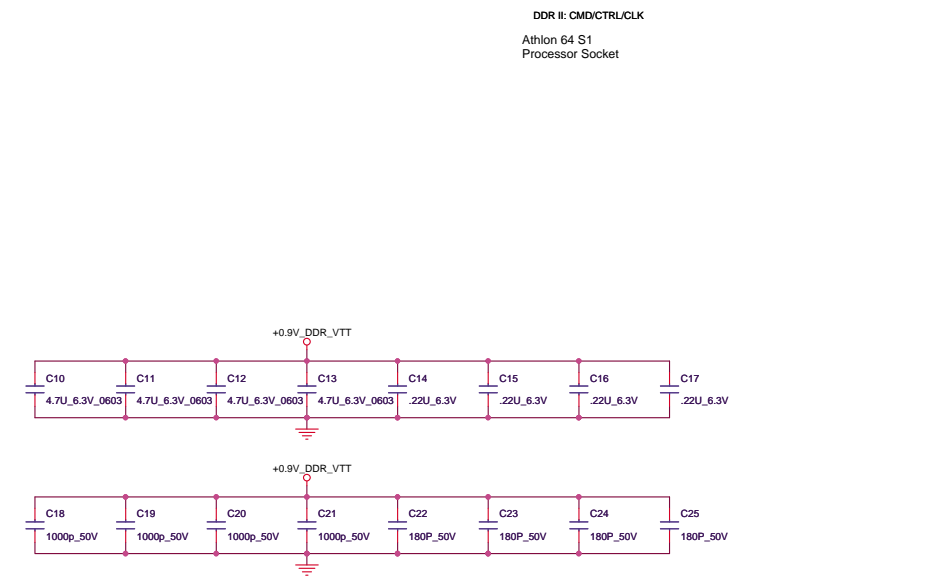
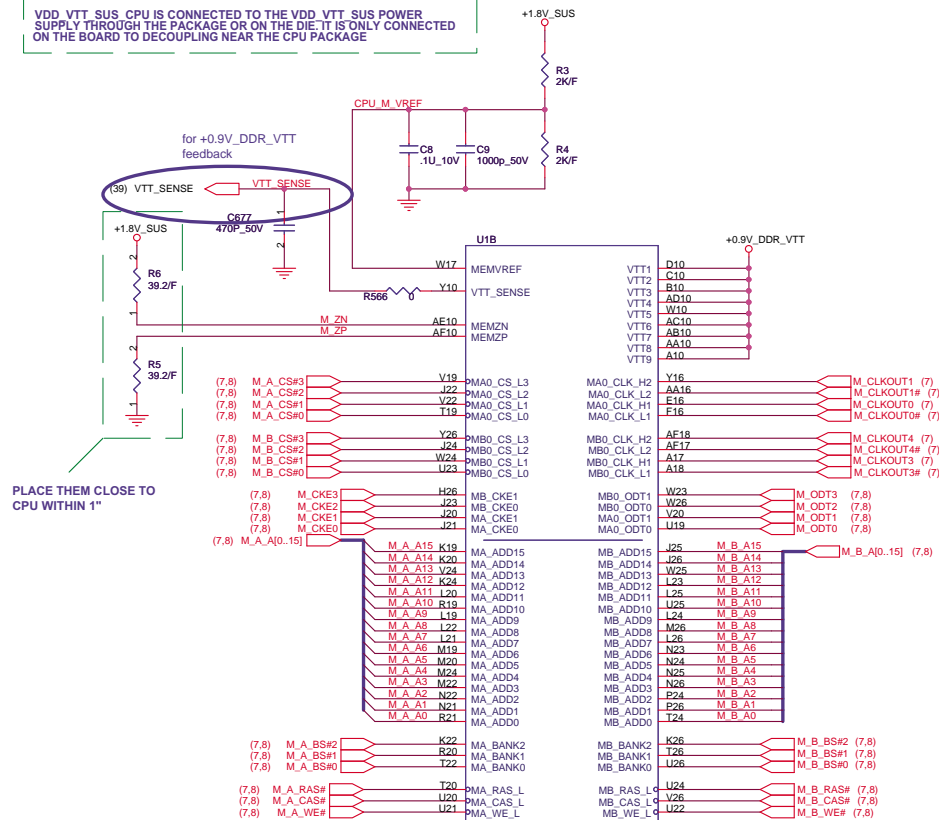
Size  
Document Number  
FX2

Date: Friday, May 05, 2006

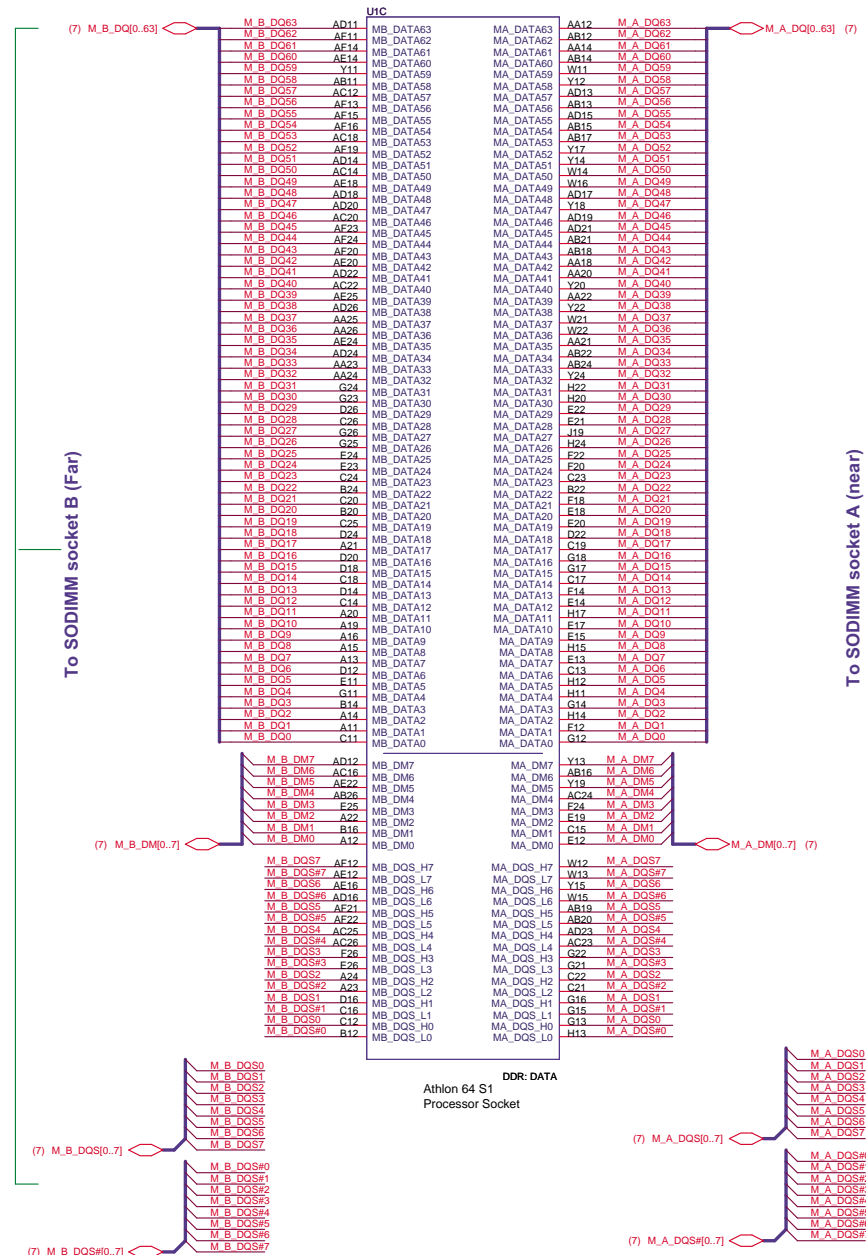
Sheet 3 of 47

Rev  
1A

VDD\_VTT\_SUS CPU IS CONNECTED TO THE VDD\_VTT\_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

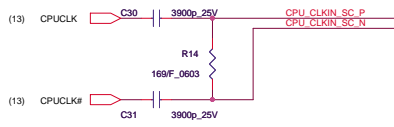
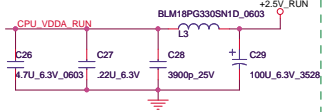


## Processor DDR2 Memory Interface

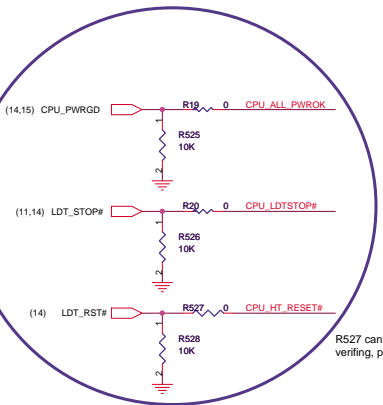


# ATHLON Control and Debug

## CPU\_VDDA\_RUN

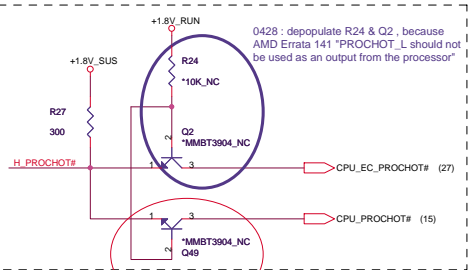


R14 close U1 within 600 mil, C30 & C31 close U1 within 1250 mil

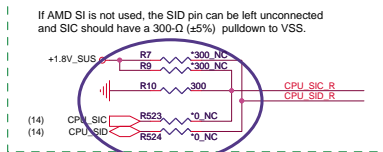


change for SB600 from SB460

R527 can be used for EMI verifying, place close to CPU



SB this pin is 3.3V, need it level-shift.



for CPU rev.F, if for rev.G, populate R7,R9,R523,R524 and depopulate R10

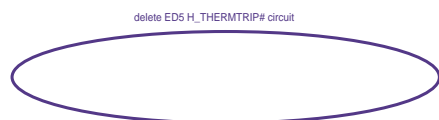
place them to CPU within 1"

To Power

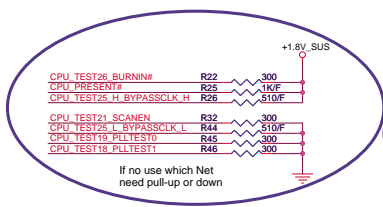
for +1.8V\_SUS feedback

add port to Page 35 U36 Thermal IC

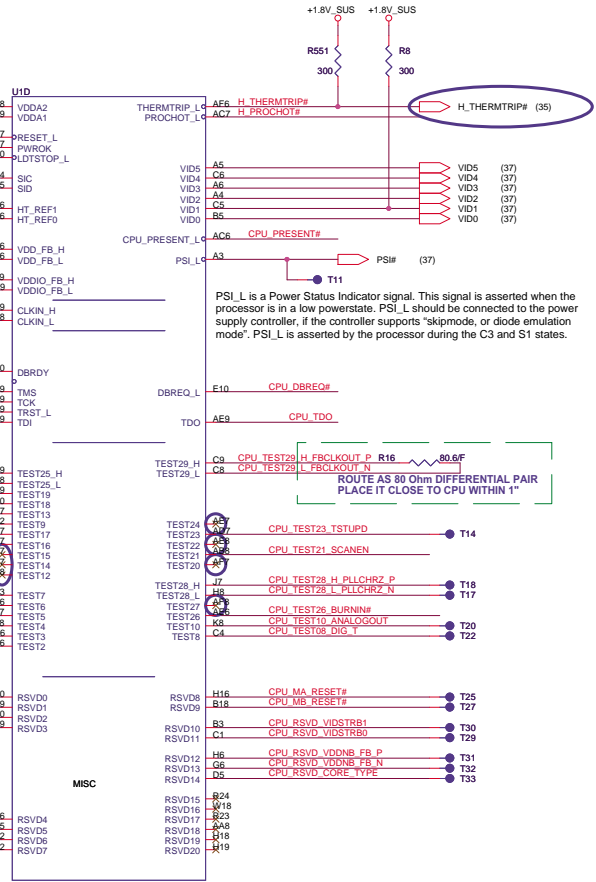
change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down



delete ED5\_H\_THERMTRIP# circuit

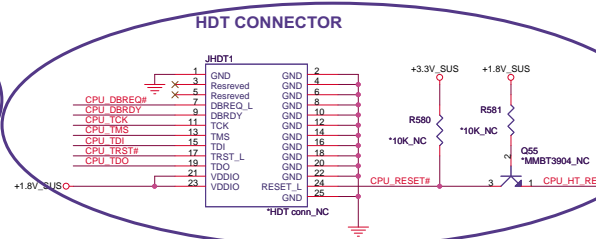


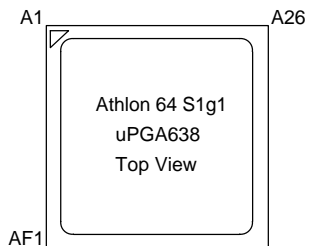
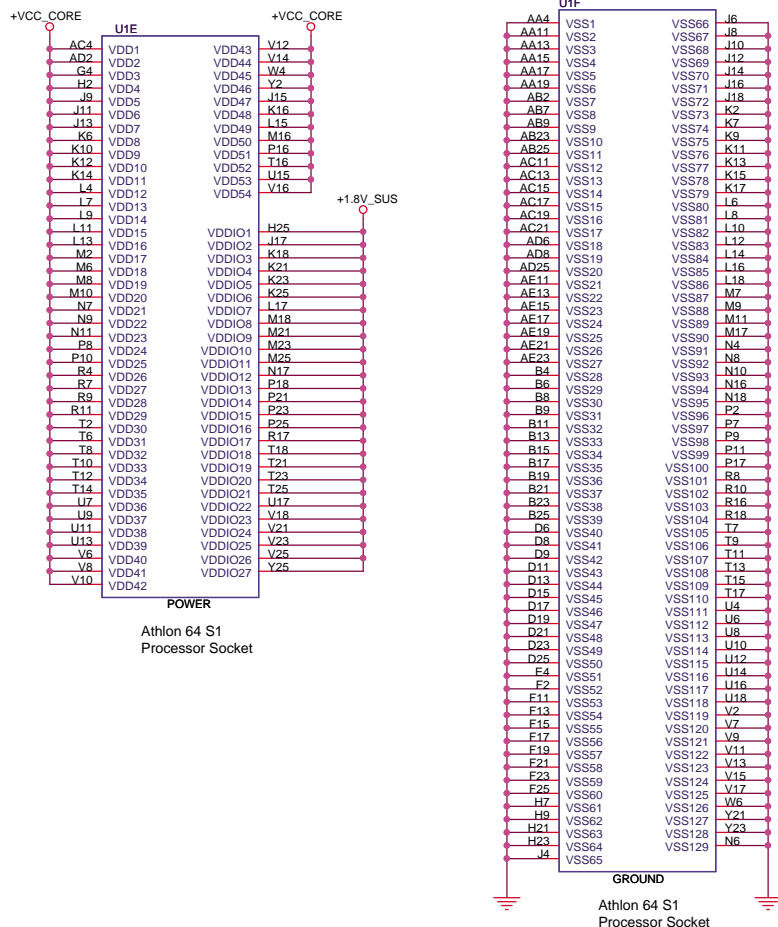
delete ED5 thermal sensor



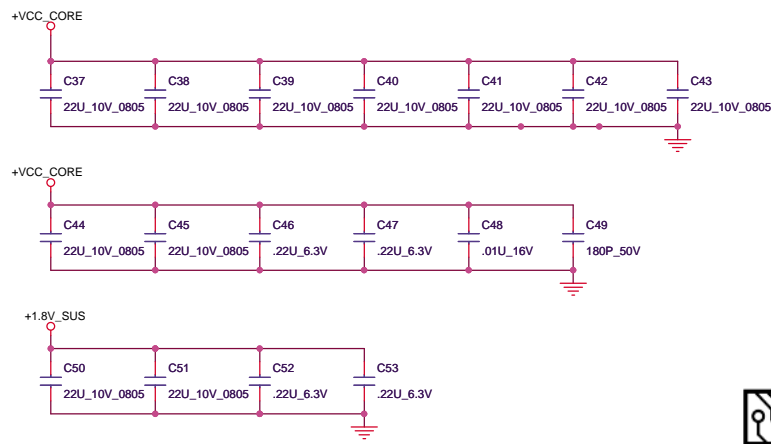
AMD NPT S1 SOCKET Processor Socket

add HDT connector for debug convenience

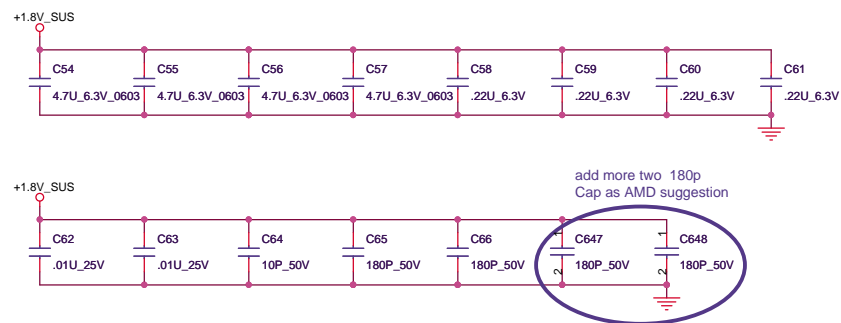




## BOTTOMSIDE DECOUPLING



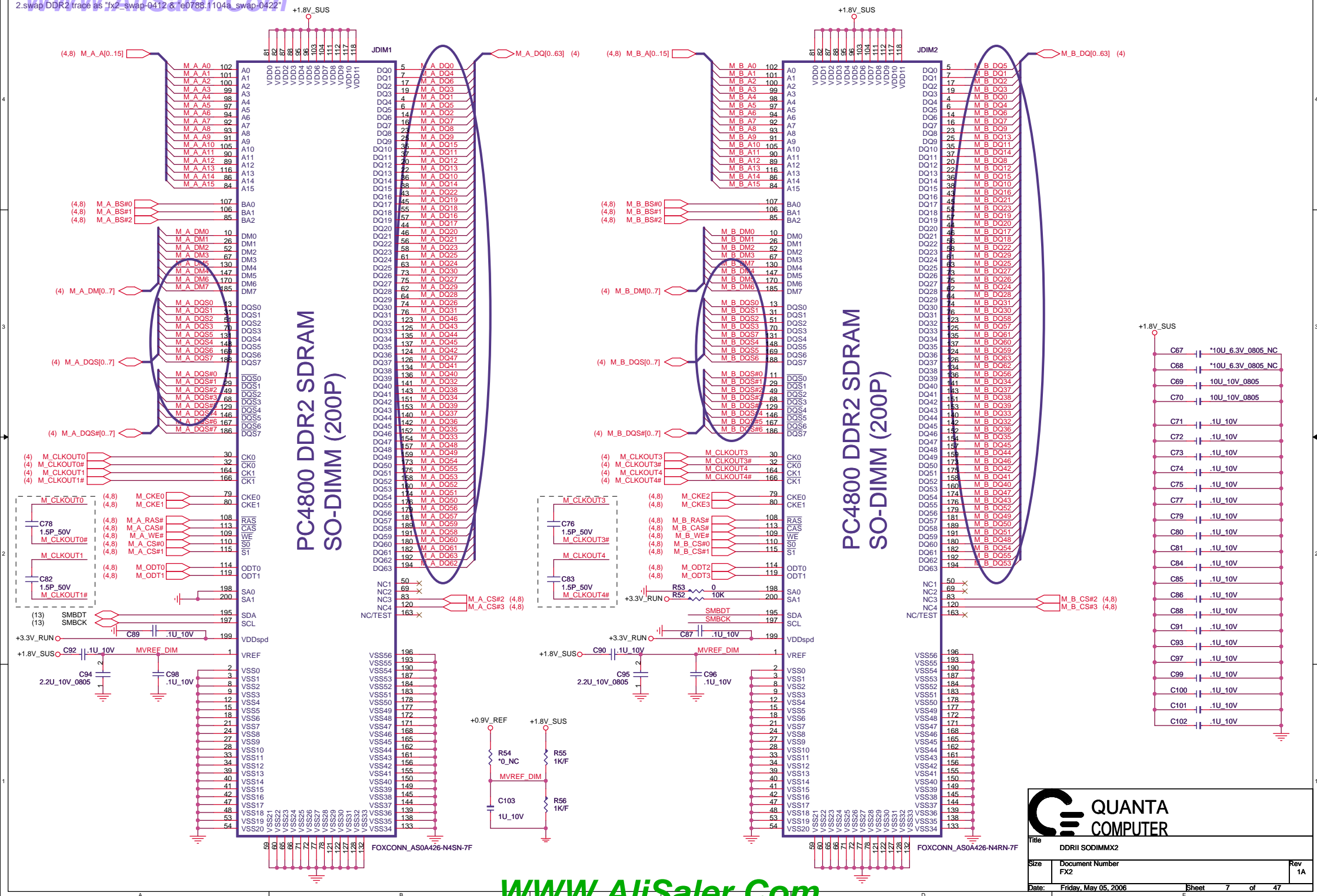
## DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE

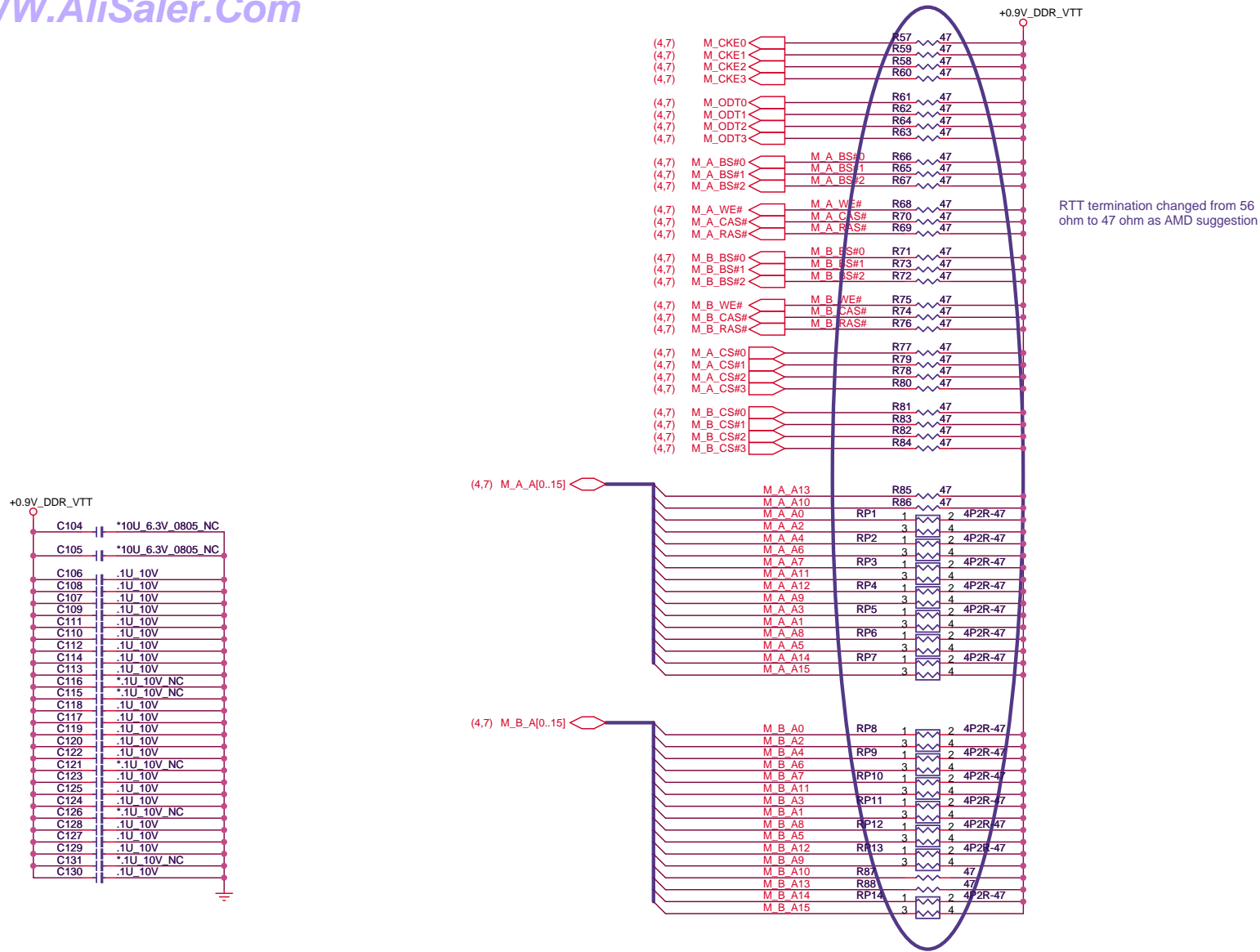


## PROCESSOR POWER AND GROUND

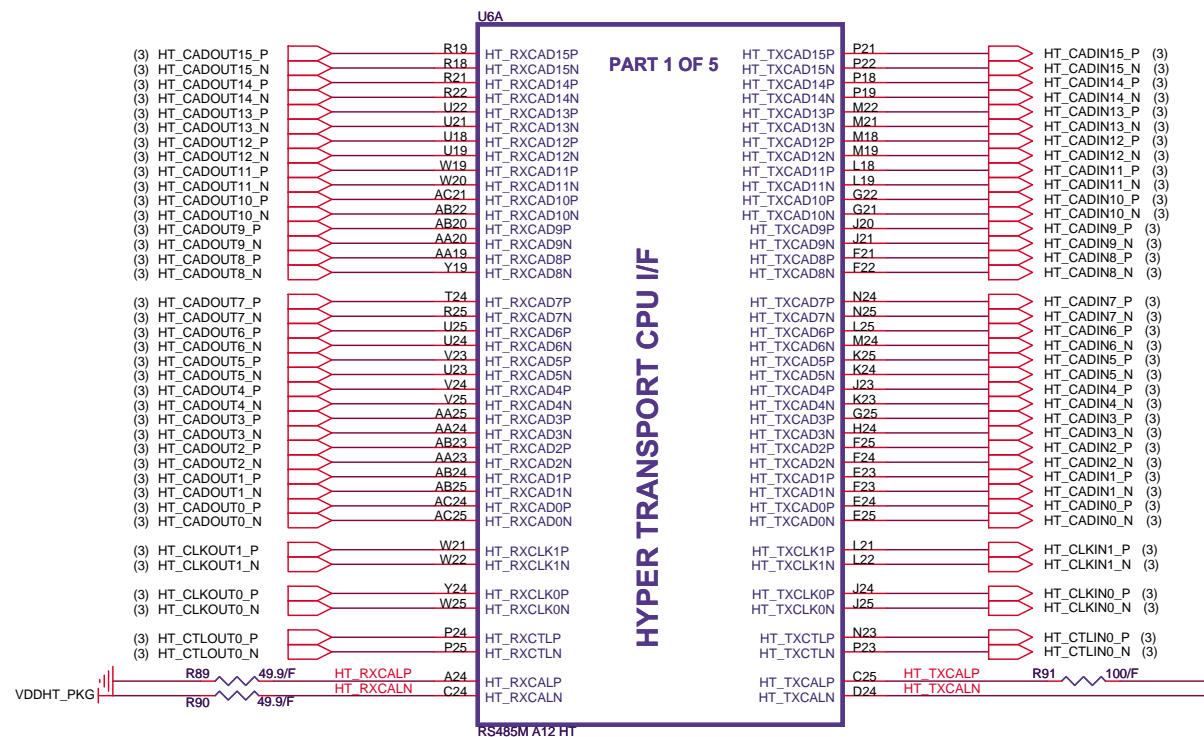


- 1.Change DDR2 socket(P/N, Description, footprint, part reference, value)
- 2.swap DDR2 trace as "fx2\_swap-0412 & "e0788.1104a\_swap-0422"







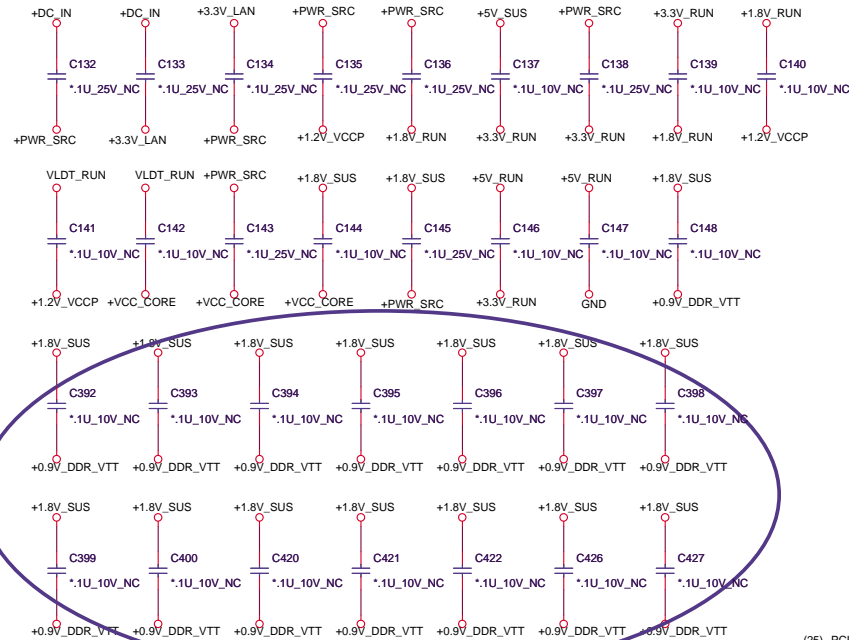


**QUANTA COMPUTER**

Title: RS485-HT LINK0 I/F

Size: Document Number FX2 Rev 1A

Date: Friday, May 05, 2006 Sheet 9 of 47



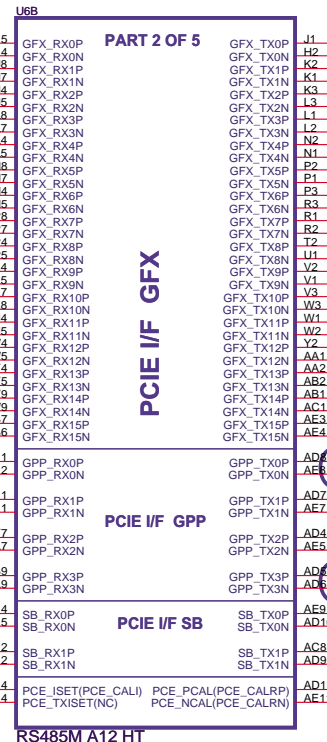
reserve more 14 Cap. between +0.9V\_DDR\_VTT & +1.8V\_SUS

delete PCIE signal , original LAN & Mini Card of ED5

(25) PCIE\_RXP1  
(25) PCIE\_RXN1  
(24) MINI\_PCIE\_RXP2  
(24) MINI\_PCIE\_RXN2

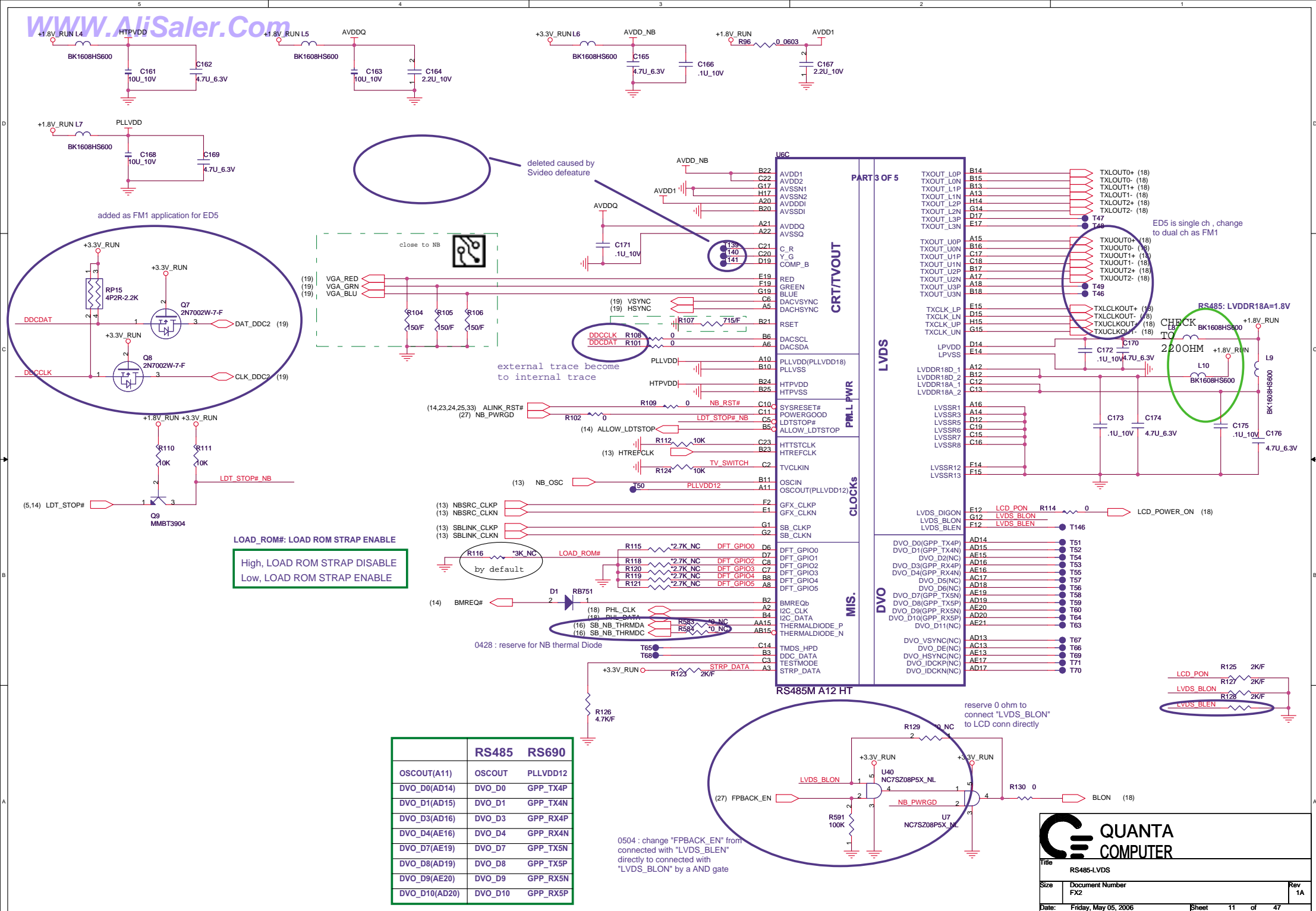
(14) A\_RX0P  
(14) A\_RX0N  
(14) A\_RX1P  
(14) A\_RX1N

R93: 10KOhm FOR RS485  
1.47KOhm FOR RS690  
R92: 8.25KOhm FOR RS485  
DNI FOR RS690

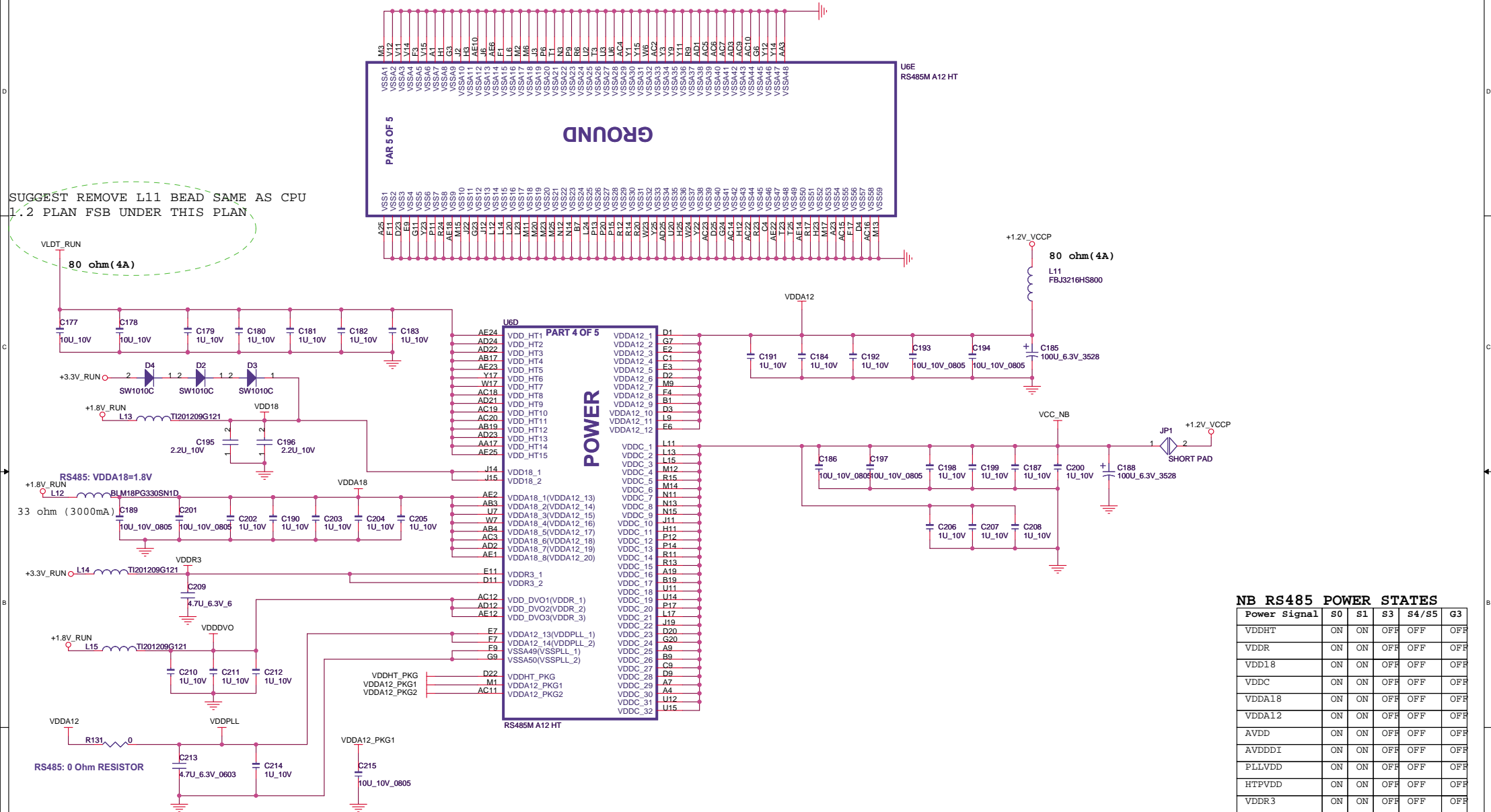


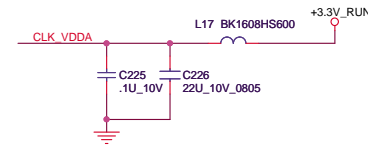
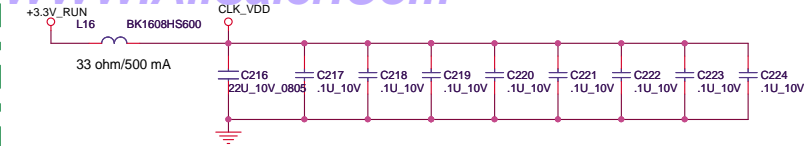
RS485M A12 HT

R95: 150 Ohm FOR RS485  
562 Ohm FOR RS690  
R94: Ward update to 100 Ohm FOR RS485  
2KOhm FOR RS690

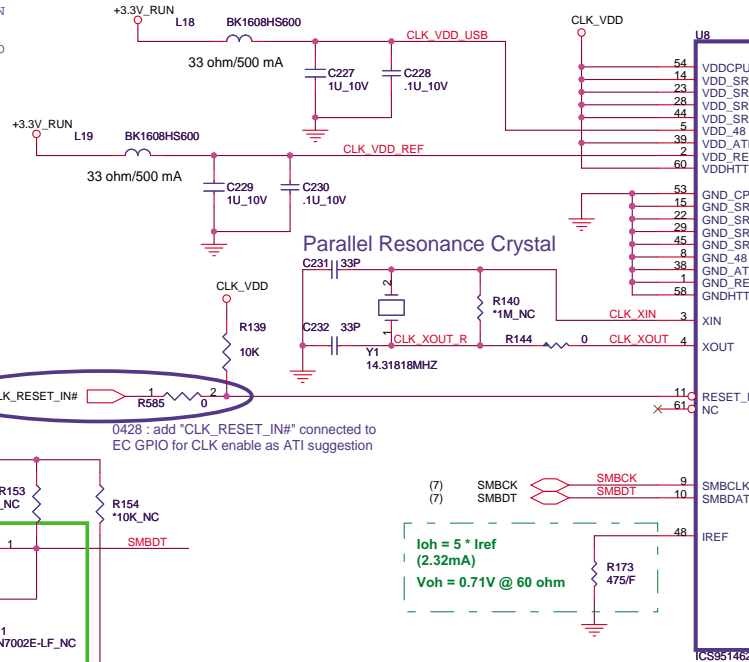


SUGGEST REMOVE L11 BEAD SAME AS CPU  
1.2 PLAN FSB UNDER THIS PLAN





- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO Clock Gen. POWER PIN



(27) CLK\_RESET\_IN#

042B: add "CLK\_RESET\_IN#" connected to EC GPIO for CLK enable as ATI suggestion

become to no used as FM1 application

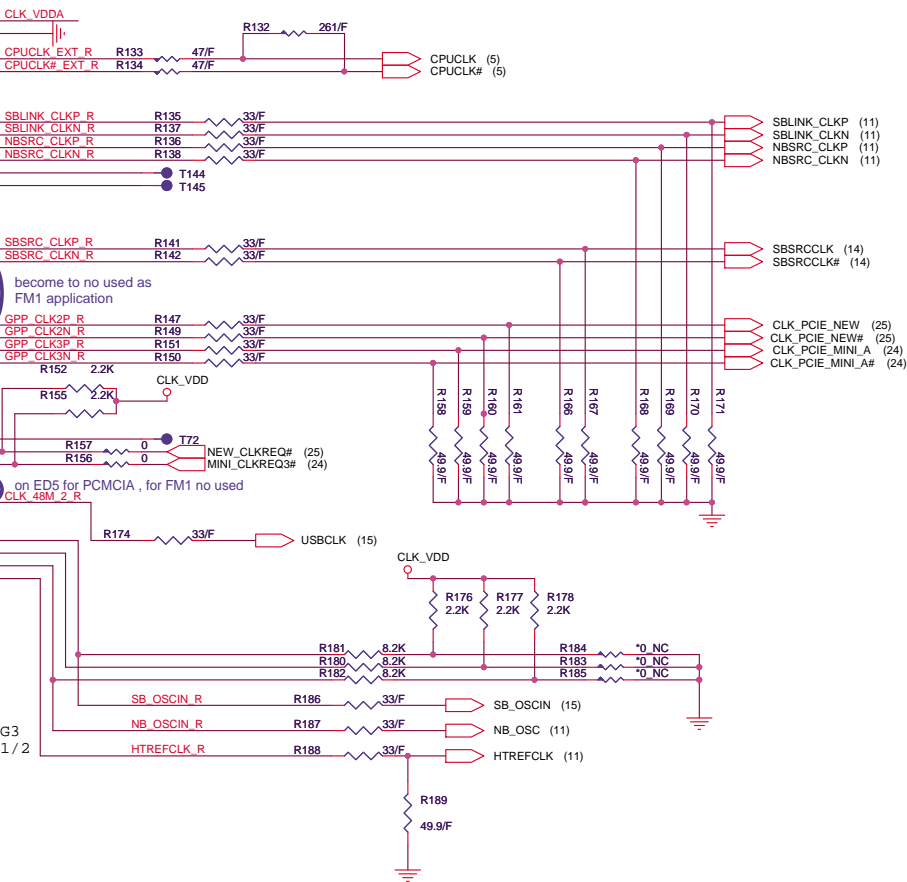
on ED5 for PCMCIA, for FM1 no used

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

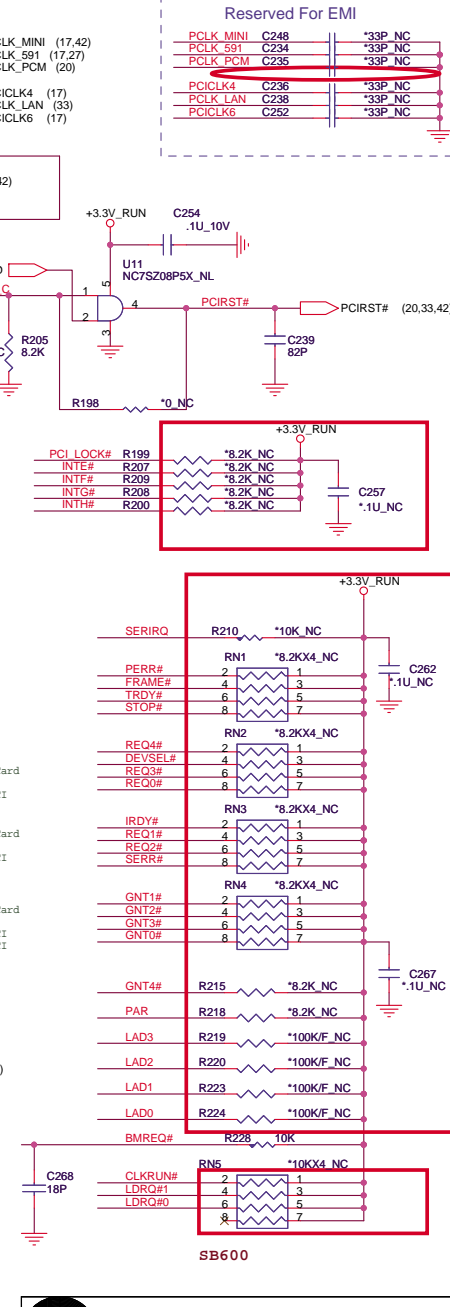
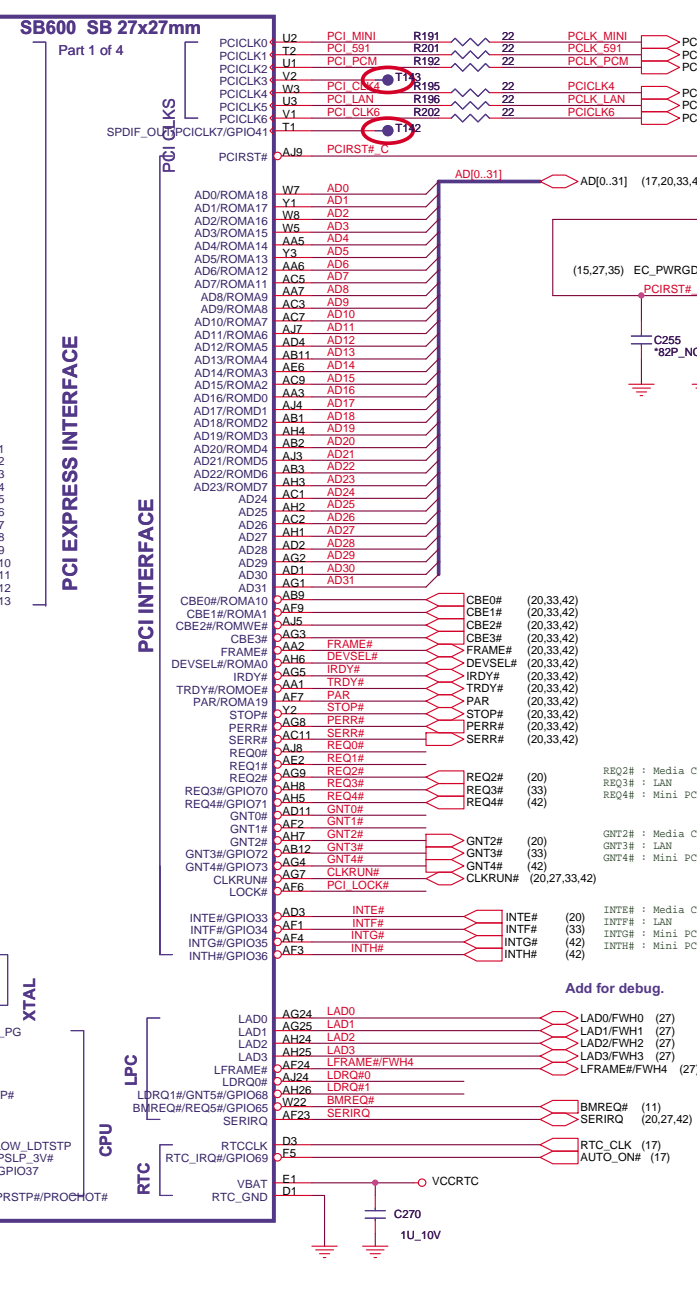
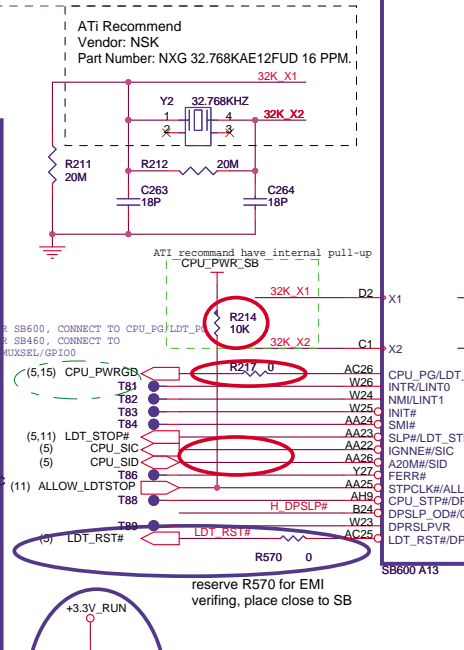
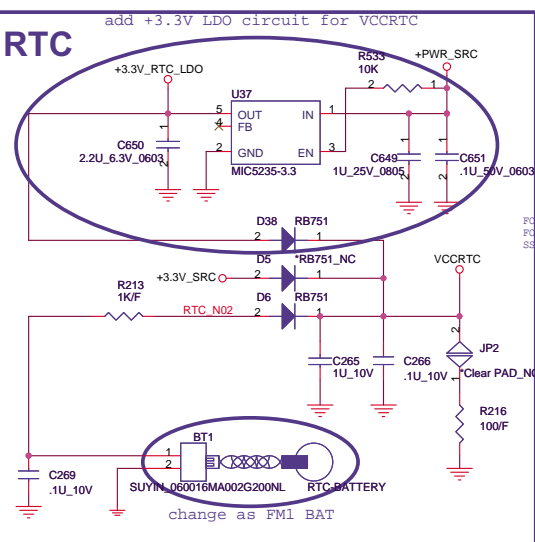
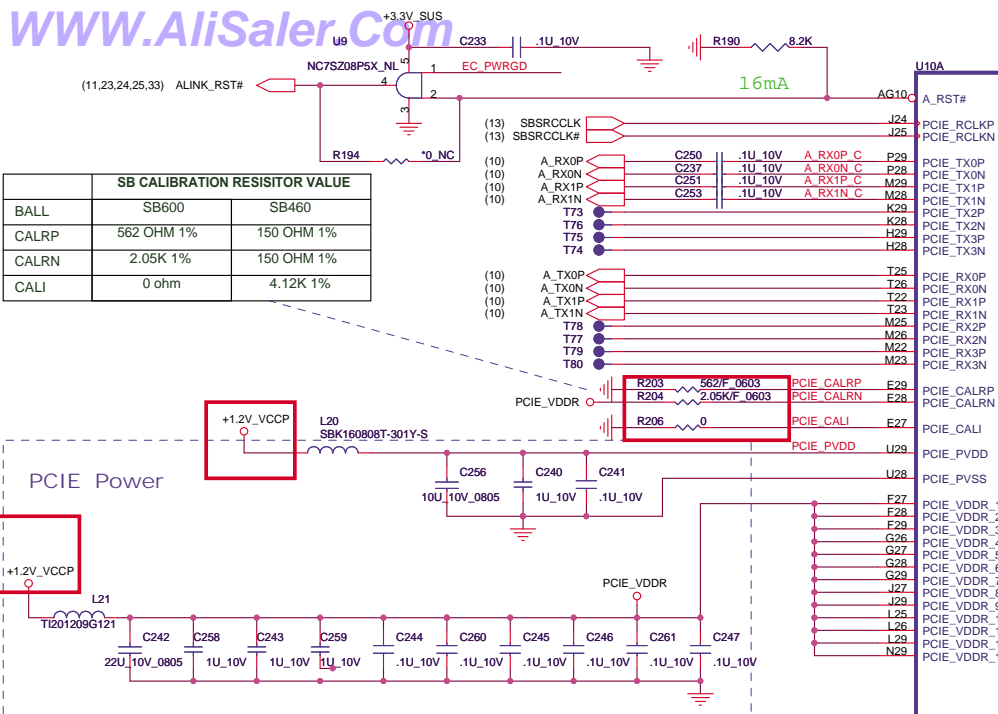
CLKREQA# CONTROL SRC5,6,7  
CLKREQB# CONTROL SRC2,3,4, ATIG3  
CLKREQC# CONTROL SRC0,1,ATIG0/1/2



QUANTA  
COMPUTER

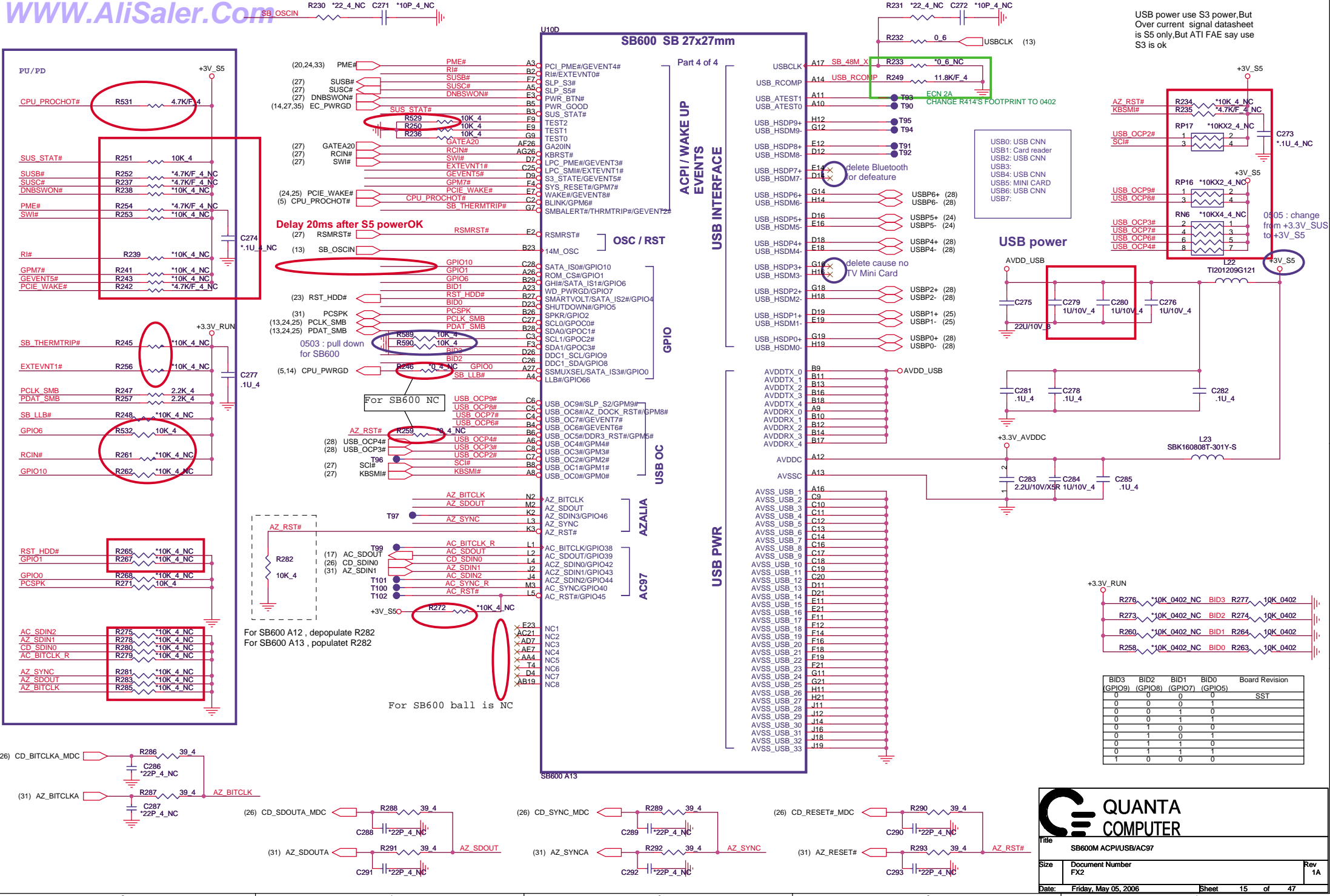
Title CLOCK GENERATOR		
Size FX2	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 13	of 47

	SB CALIBRATION RESISTOR VALUE	
BALL	SB600	SB460
CALRP	562 OHM 1%	150 OHM 1%
CALRN	2.05K 1%	150 OHM 1%
CALI	0 ohm	4.12K 1%



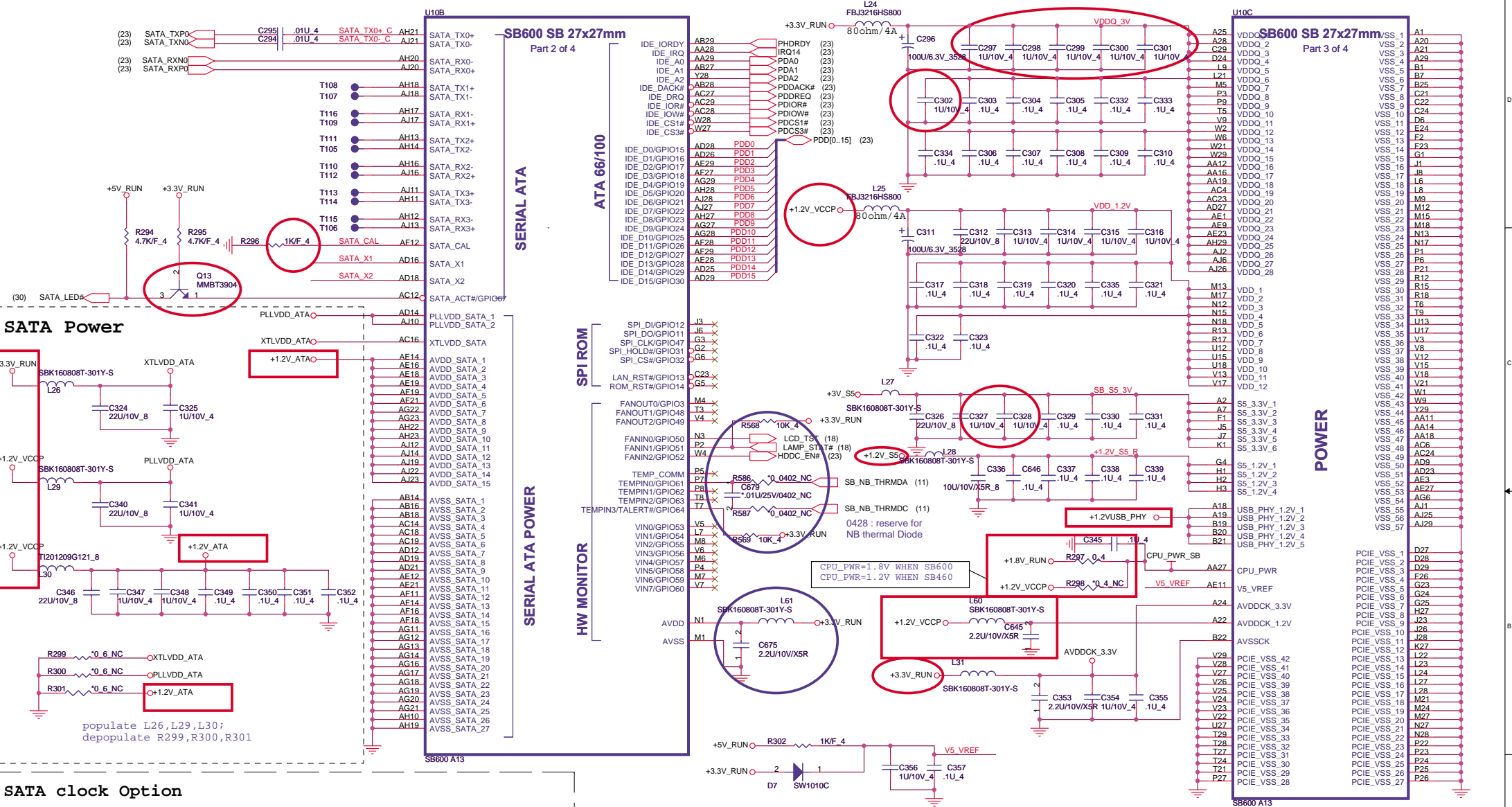
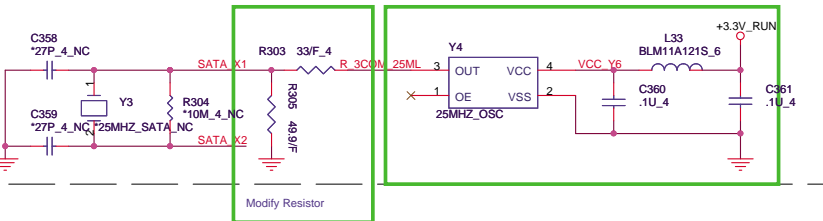
Title		SB600M-PCIE/PCM.LPC	
Size	Document Number	Revision	
	FX2		
Date	Friday, May 05, 2006	Sheet	14 of 47



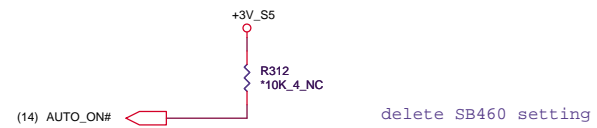
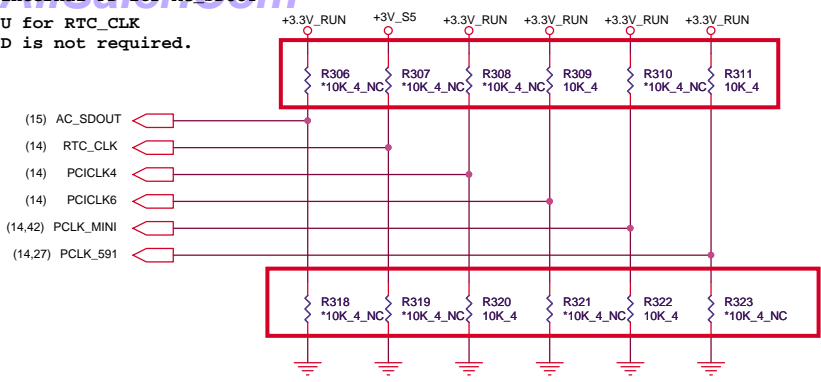




## SATA clock Option

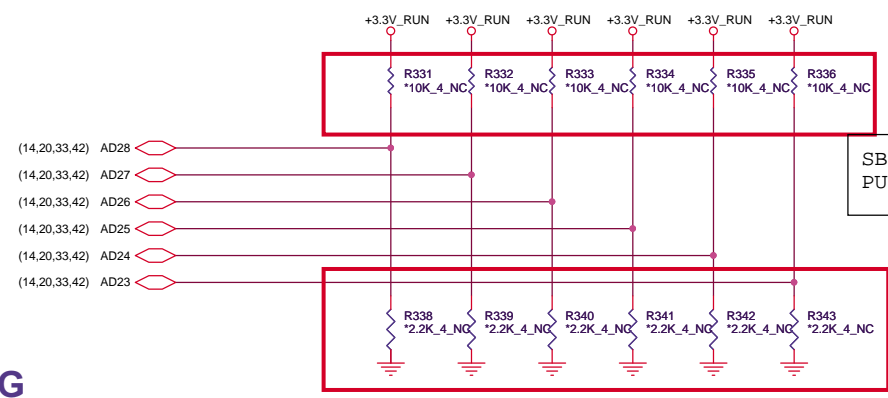
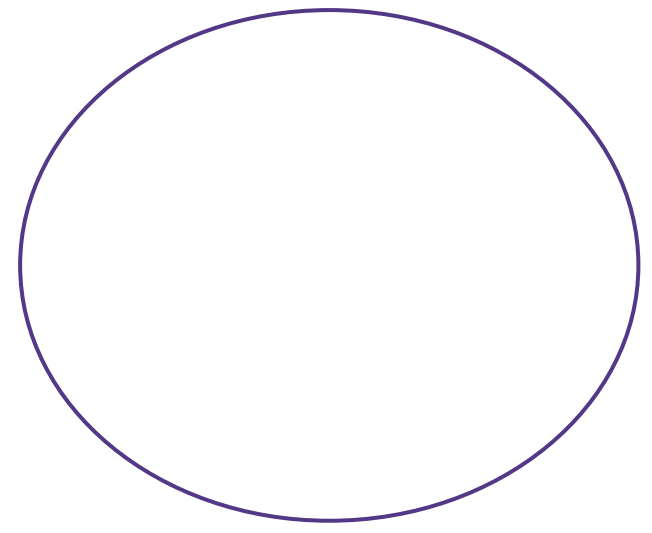


SB600 has 15K internal PD for AC\_SDOUT  
15K internal PU for RTC\_CLK  
,External PU/PD is not required.



## REQUIRED STRAPS

						PCLK_MINI	PCLK_591
PULL HIGH	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1	
	USE DEBUG STRAPS DEFAULT	INTERNAL RTC DEFAULT	USE INT. PLL48 DEFAULT	CPU IF=K8 DEFAULT	H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4			



SB600 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]


## DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Use Long Reset DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	boot fail time disabled DEFAULT
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled

SB460 Only

SB600 Only

SB600 Only

**QUANTA  
COMPUTER**

TitleSB600M STRAPS

SizeDocument NumberFX2Rev1A

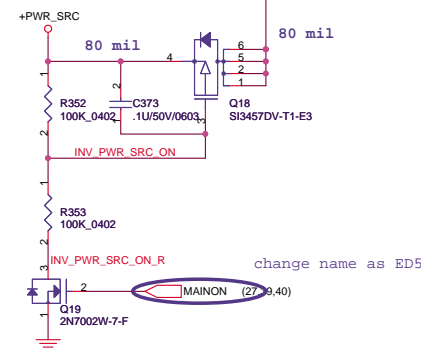
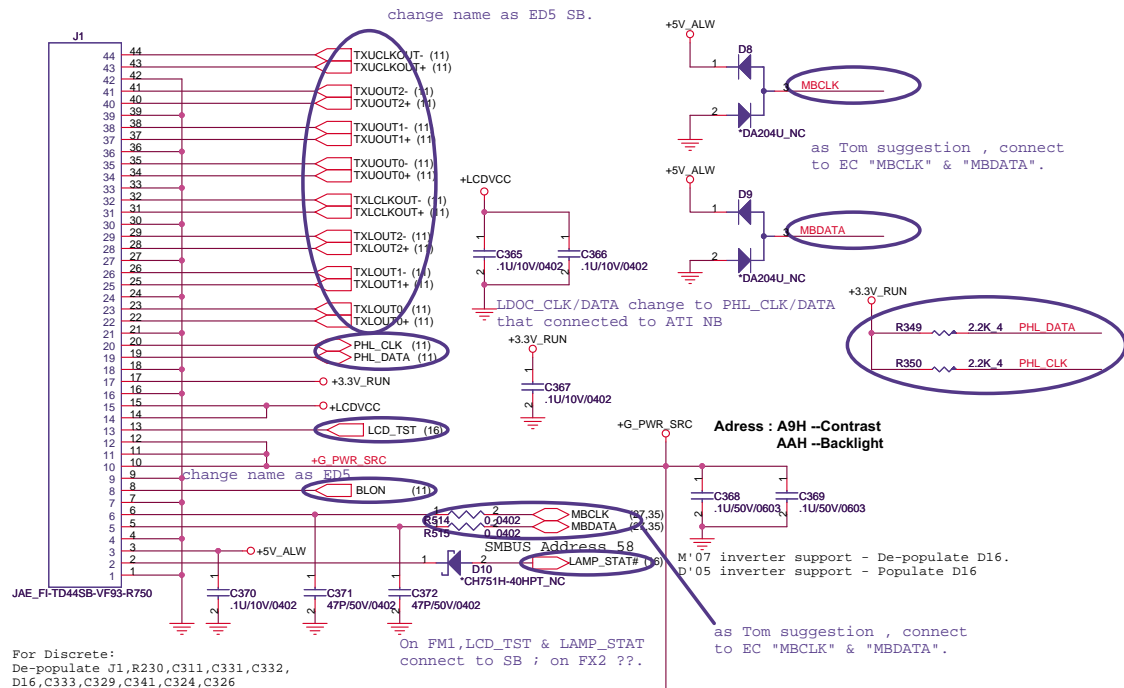
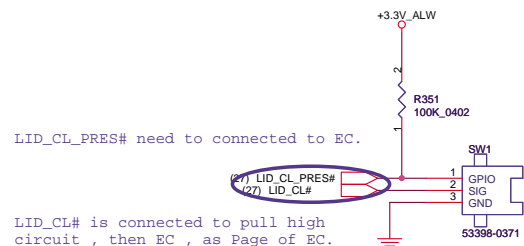
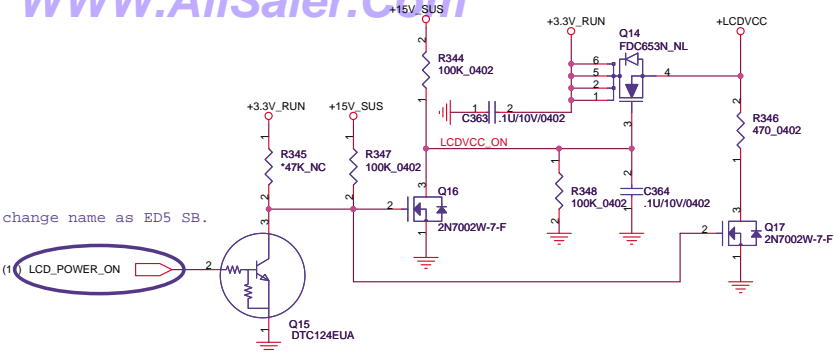
Date:Friday, May 05, 2006Sheet17 of 47

change name as ED5 SB.

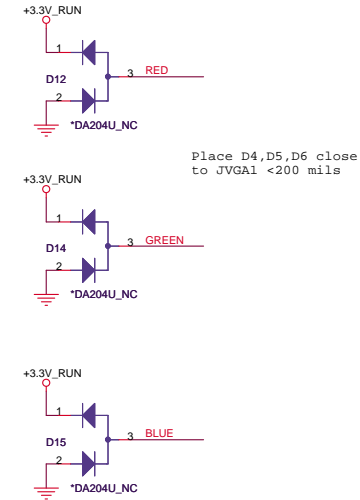
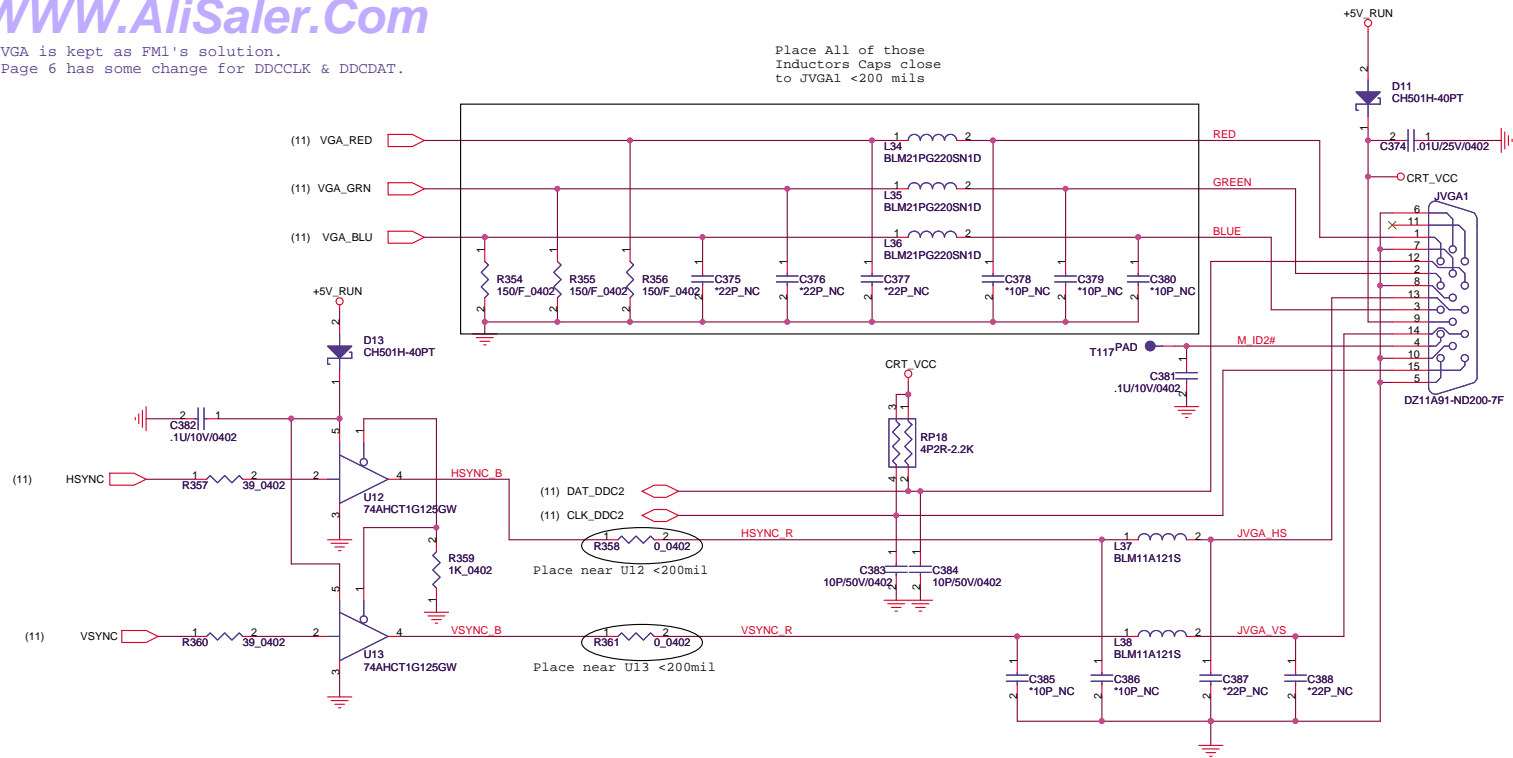
(1) LCD\_POWER\_ON

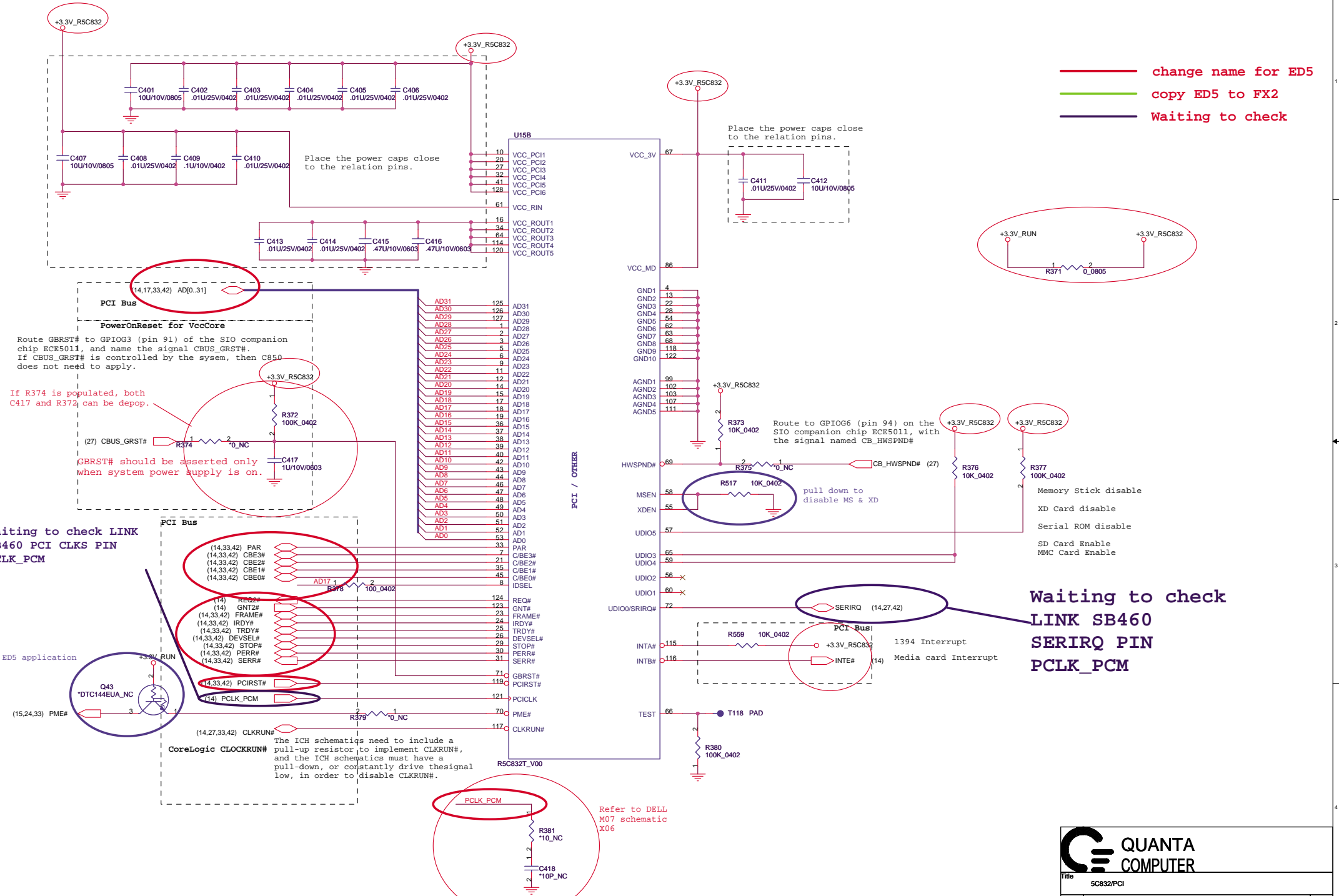
LID\_CL\_PRES# need to connected to EC.

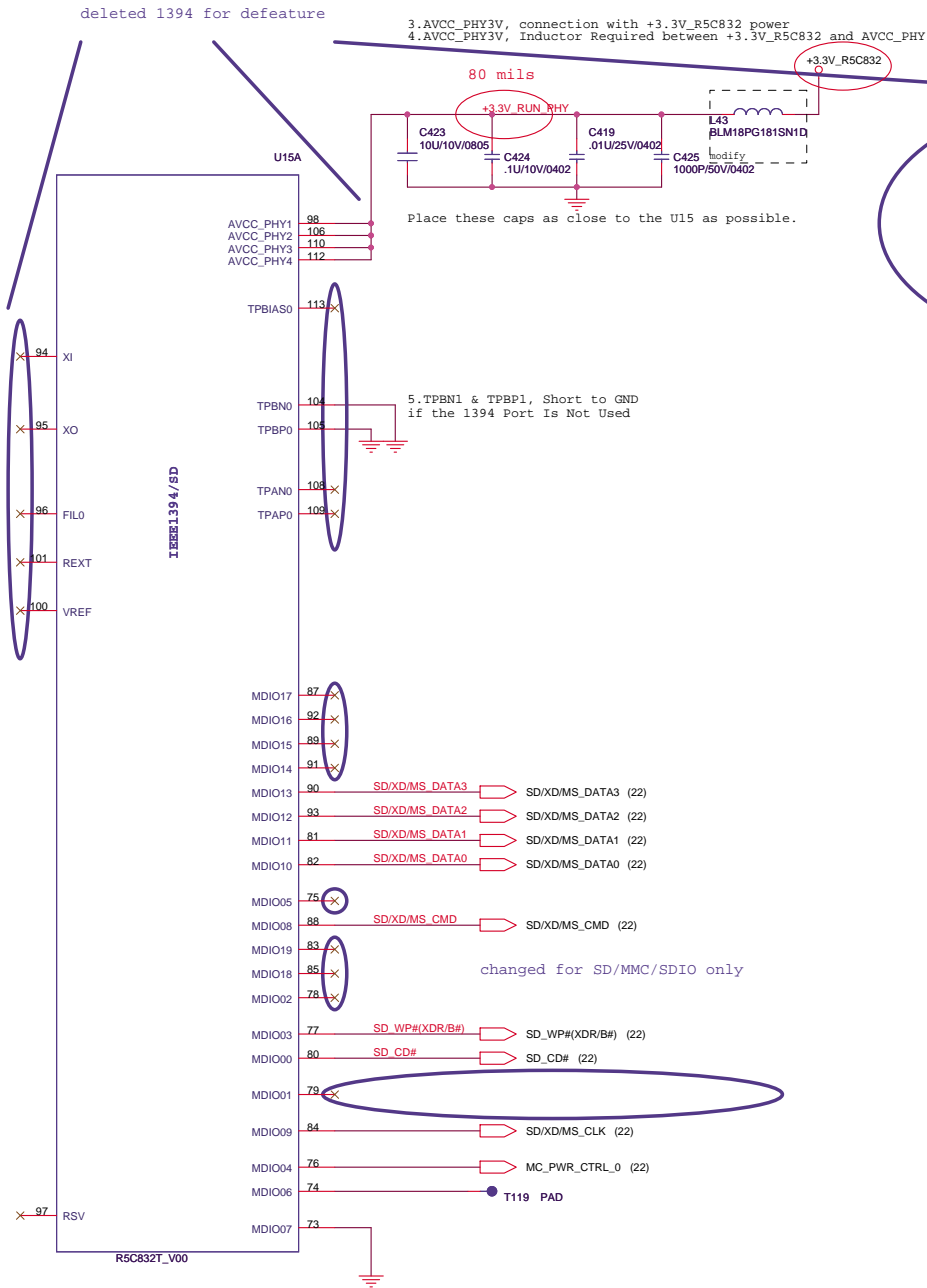
LID\_CL# is connected to pull high circuit , then EC , as Page of EC.



Place All of those  
Inductors Caps close  
to JVGAI <200 mils

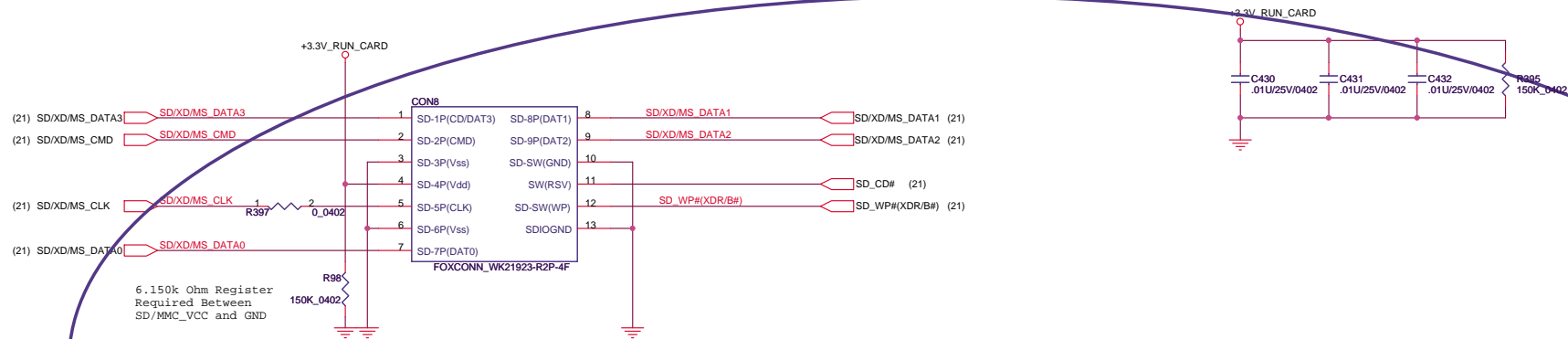






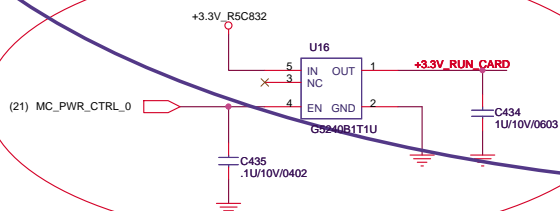
DO NOT INSERT SD/MMC SIMULTANEOUSLY.

changed for SD/MMC/SDIO only



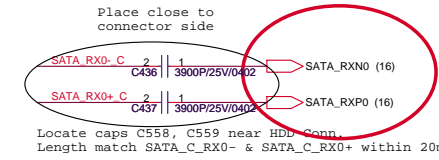
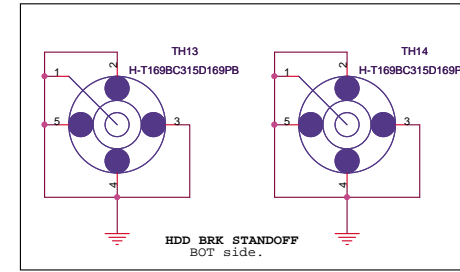
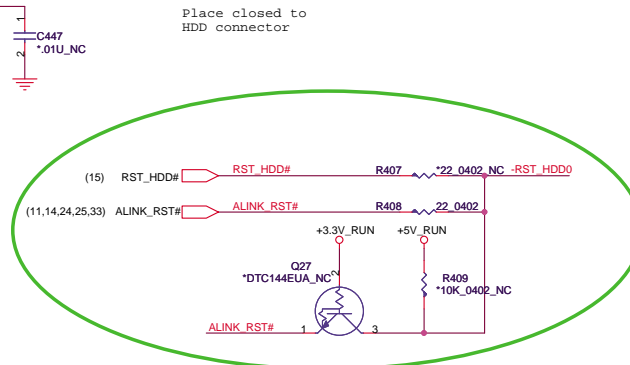
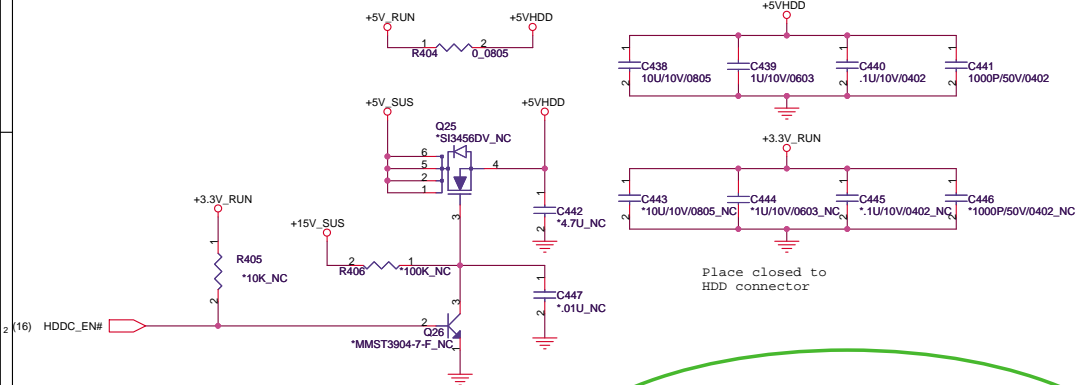
### 3 IN 1 CARD READER

For SD/MS power



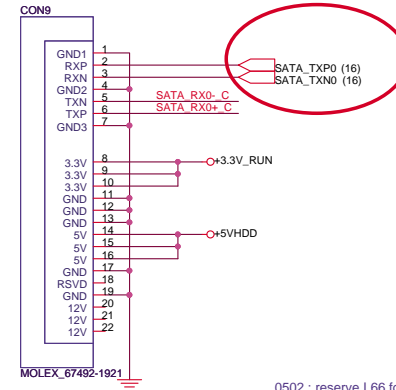


## SATA HDD



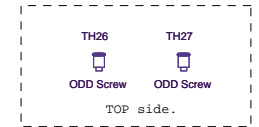
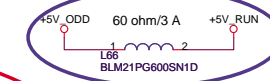
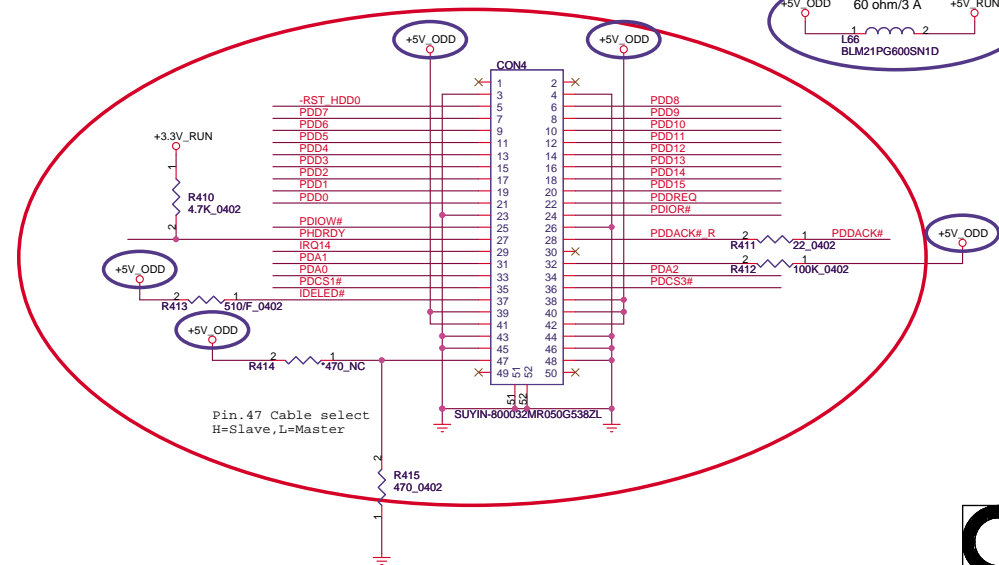
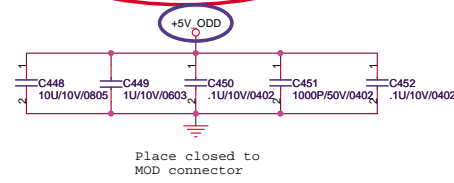
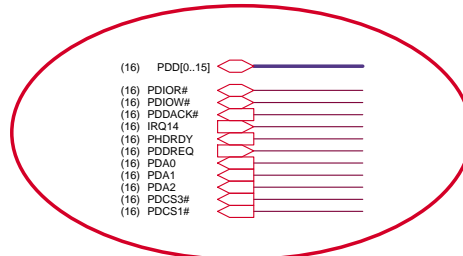
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:  
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.



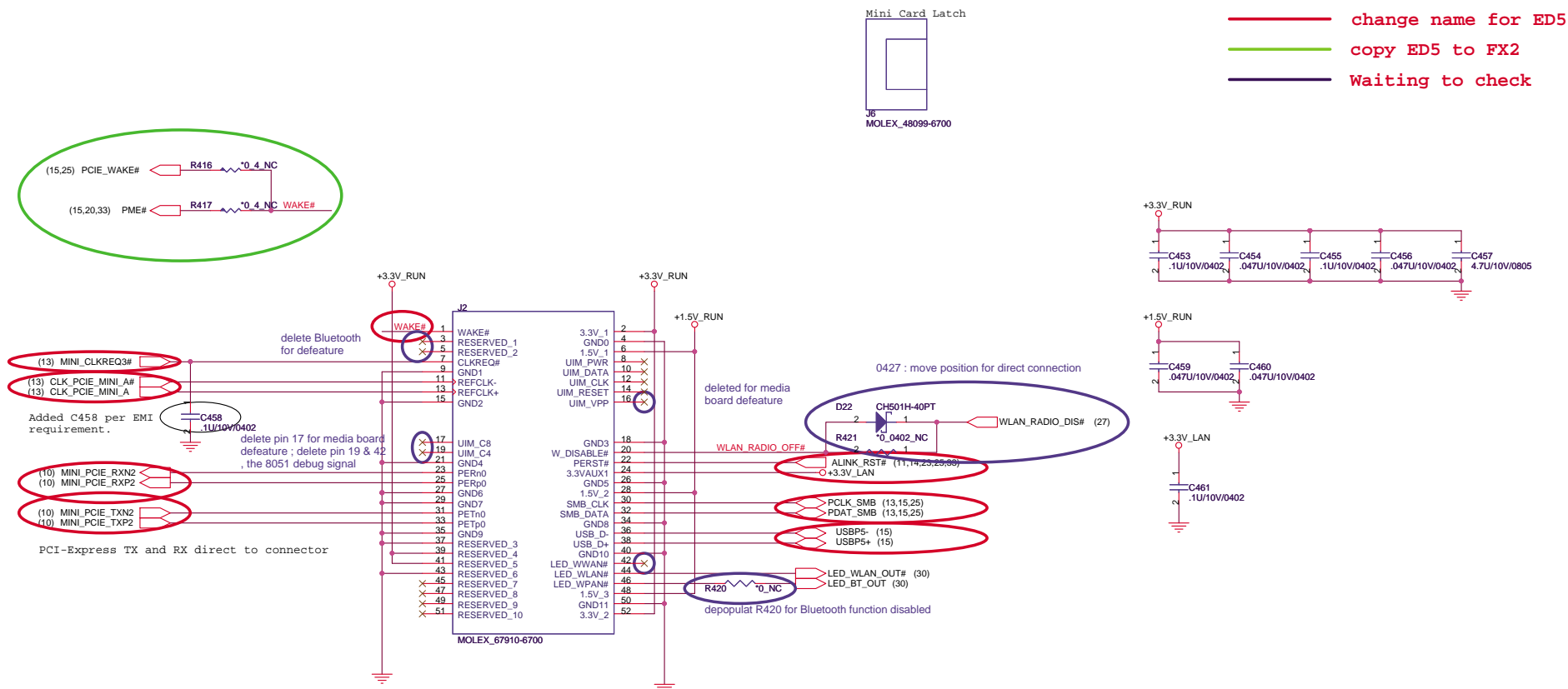
- change name for ED5
- copy ED5 to FX2
- Waiting to check

## PATA ODD

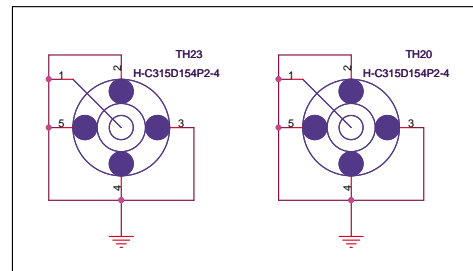


Title			SATA HDD & PATA ODD	
Size	Document Number	Rev		
	FX2	1A		
Date:	Friday, May 05, 2006	Sheet	23	of 47

## MINI CARD

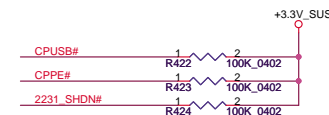
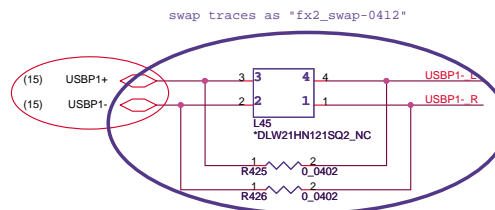
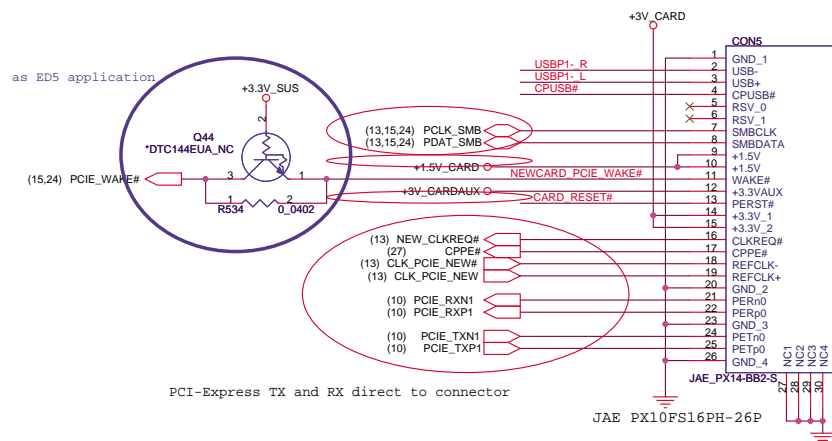


# Express Card

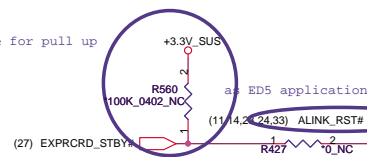


- change name for ED5
- copy ED5 to FX2
- Waiting to check

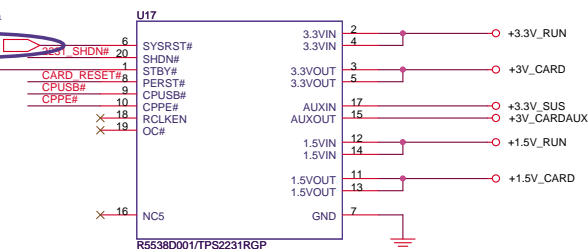
NEW CARD GUIDE POST  
TOP side.



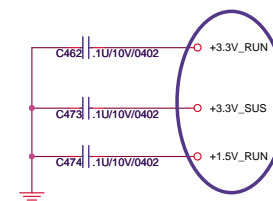
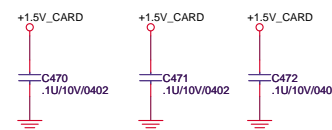
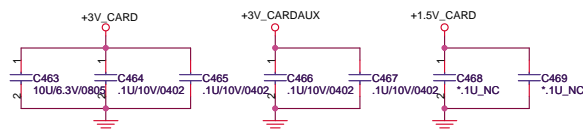
reserve for pull up



+1.5V\_CARD Max. 650mA, Average 500mA  
+3V\_CARD Max. 1300mA, Average 1000mA

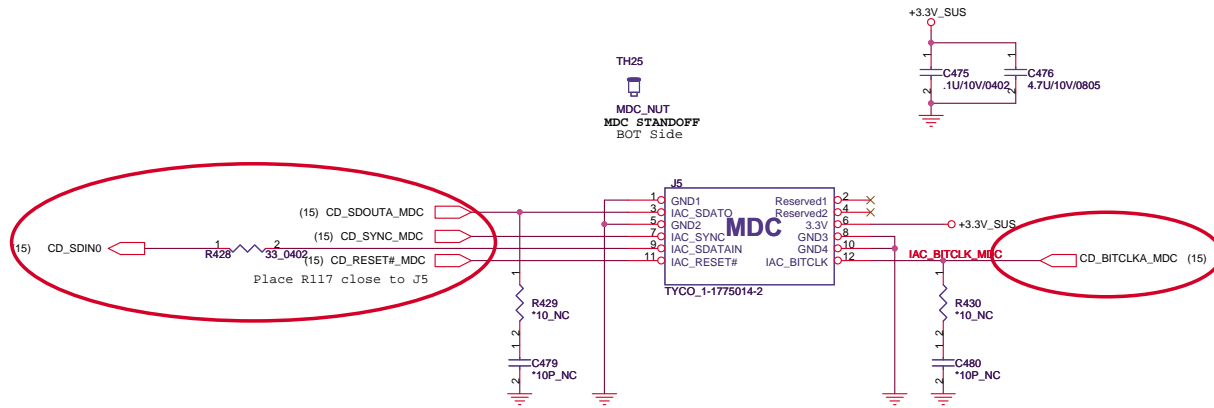


+1.5V\_CARD Max. 650mA, Average 500mA  
+3V\_CARD Max. 1300mA, Average 1000mA

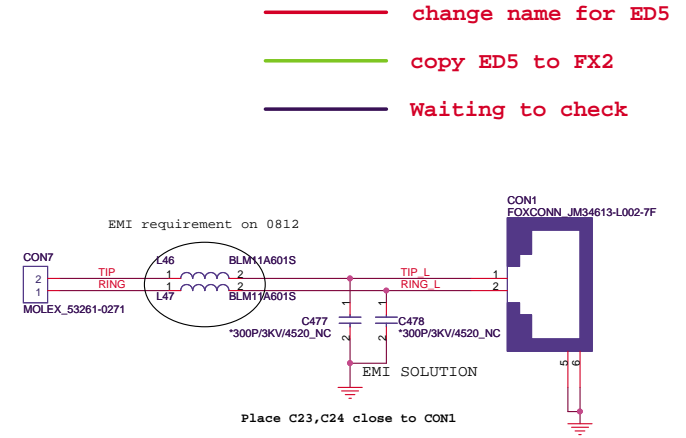


Express Card		
Size	Document Number	Rev
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Date:	Friday, May 05, 2006	Sheet 25 of 47

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG  
(stranded or twisted pair wire)



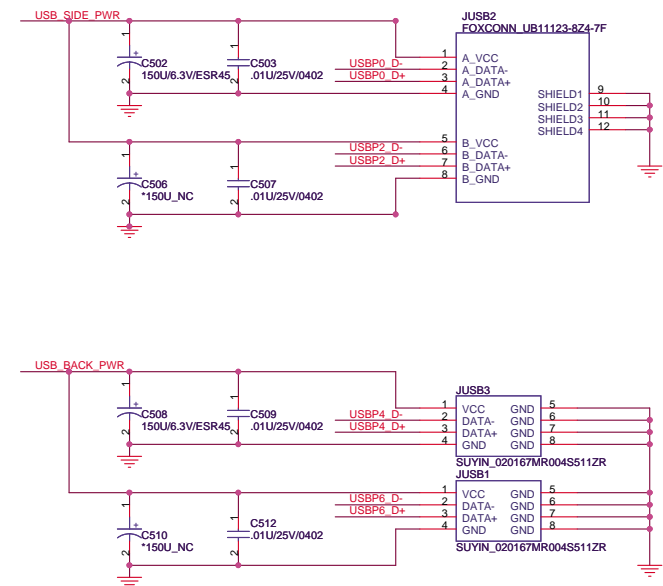
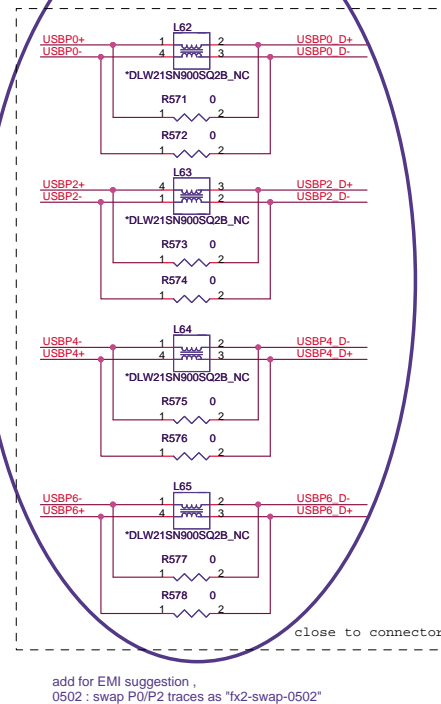
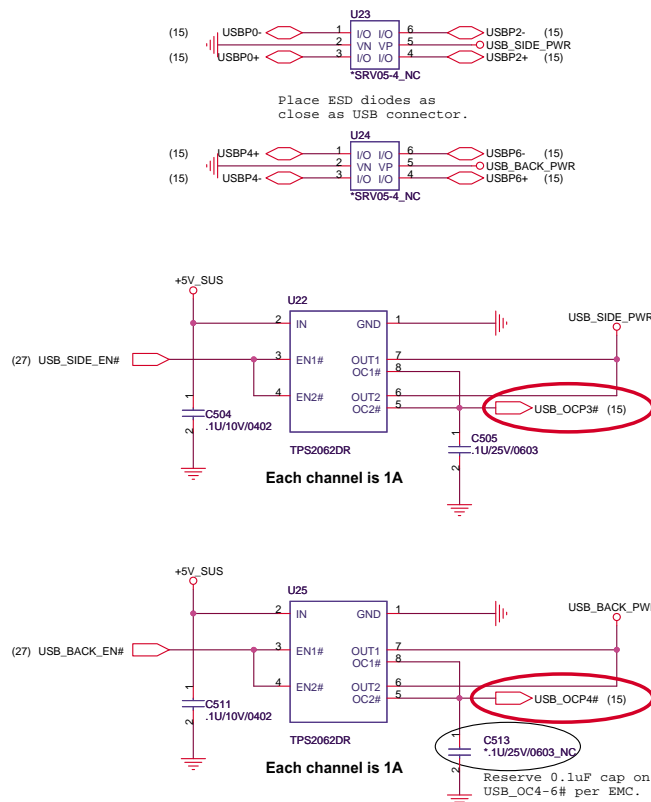
```
delete Bluetooth
for defeature
```

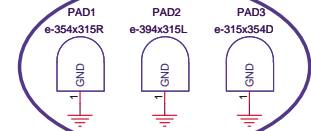




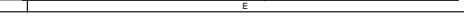
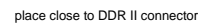
8Mbit (1M Byte), SPI

- change name for ED5
- copy ED5 to FX2
- Waiting to check

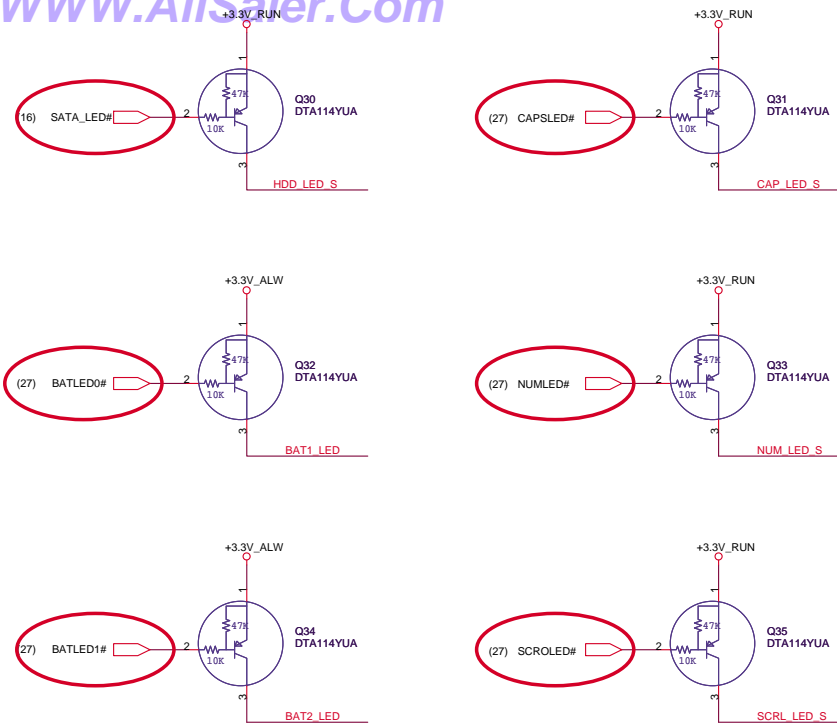




0505 : delete PV12 , caused interference with power component , EMI confirm no concern

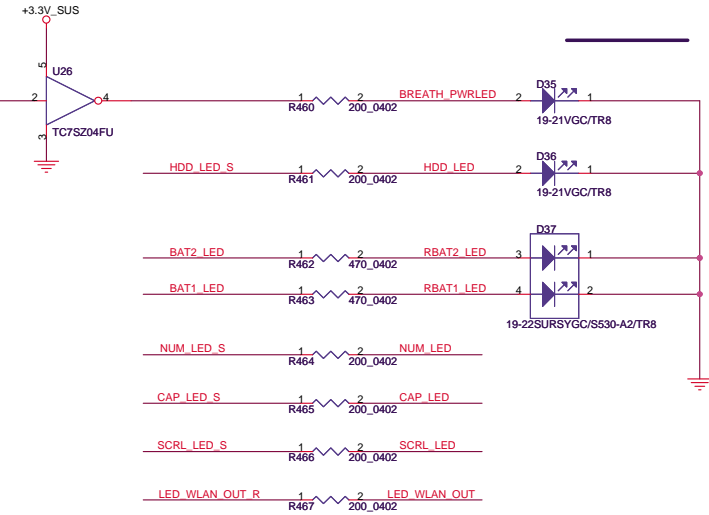




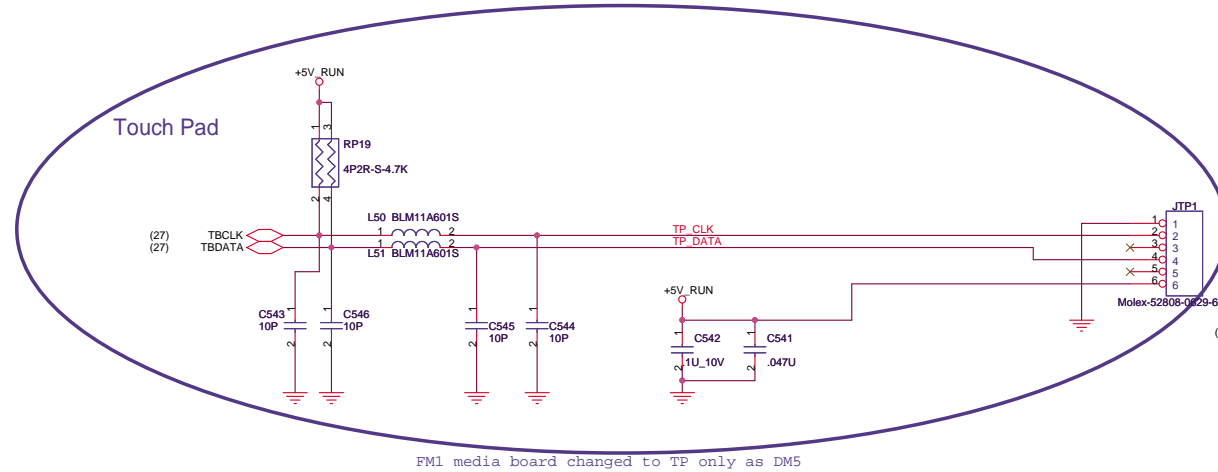


0427 : change from  
BREATH\_LED to BREATH\_LED#

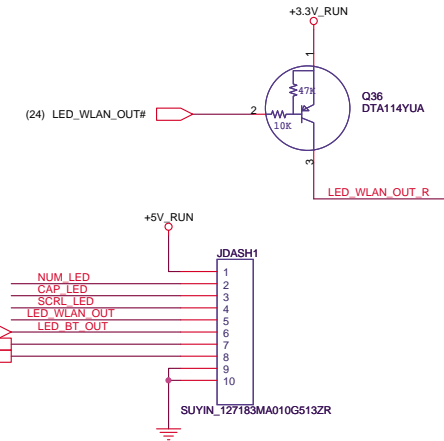
(27) BREATH\_LED#

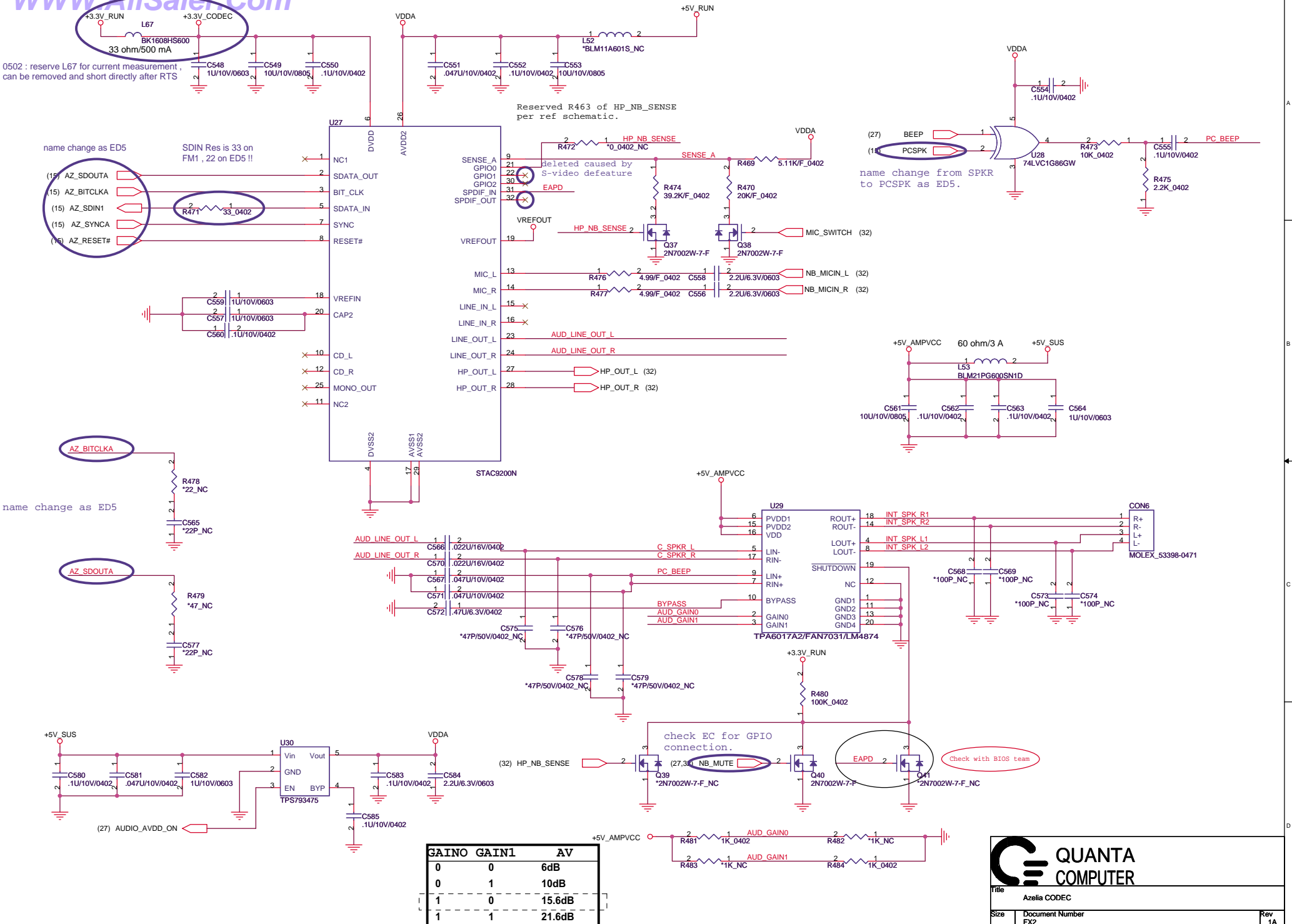


change name for ED5  
copy ED5 to FX2  
Waiting to check



FM1 media board changed to TP only as DM5





**QUANTA COMPUTER**

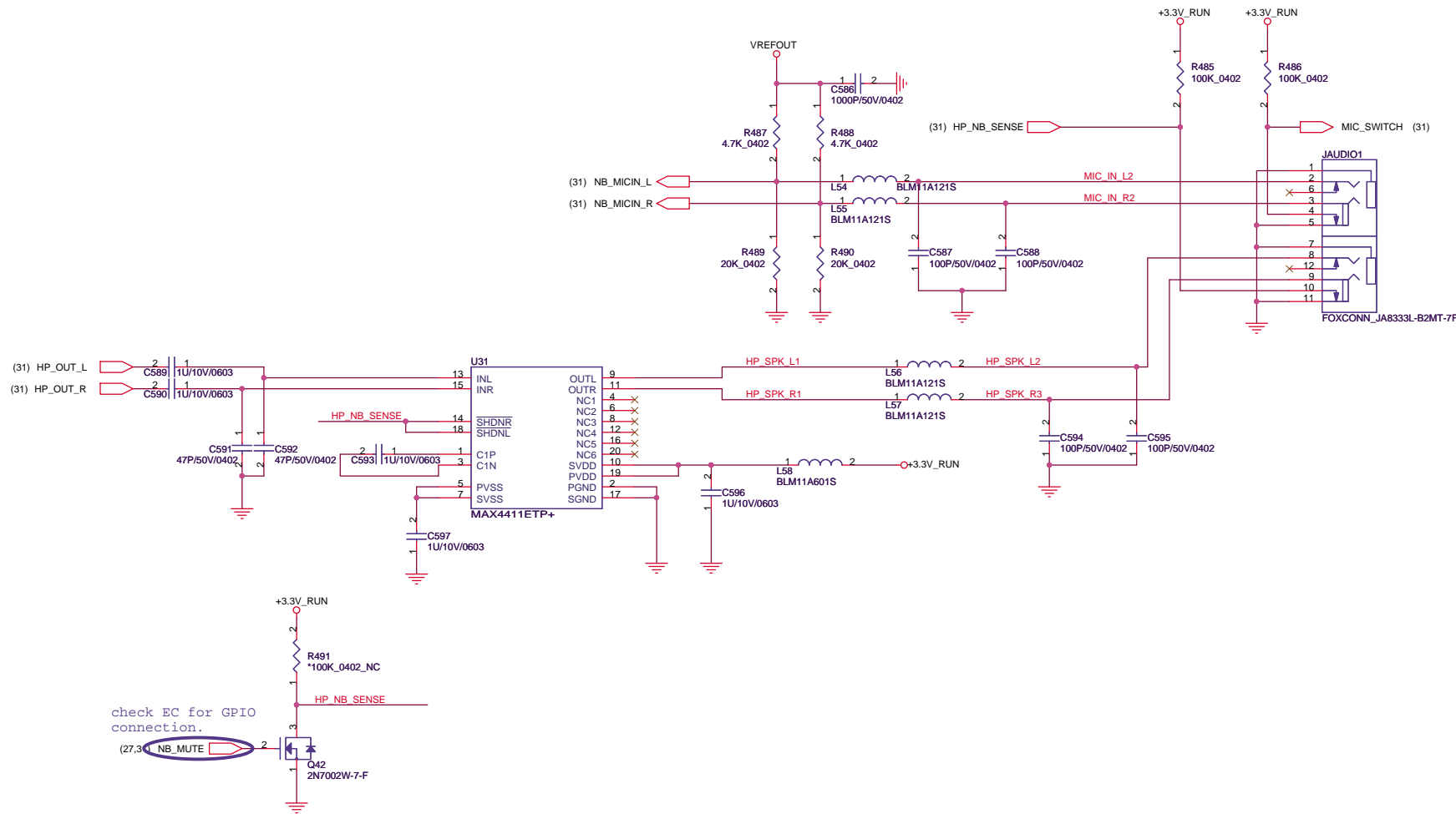
Title: Azelia CODEC

Size: Document Number FX2

Date: Friday, May 05, 2006

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Rev 1A



Title		
AUDIO CONN		
Size	Document Number	Rev
FX2		1A
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- change name for ED5
- copy ED5 to FX2
- Waiting to check

[illegible]

K\_0402

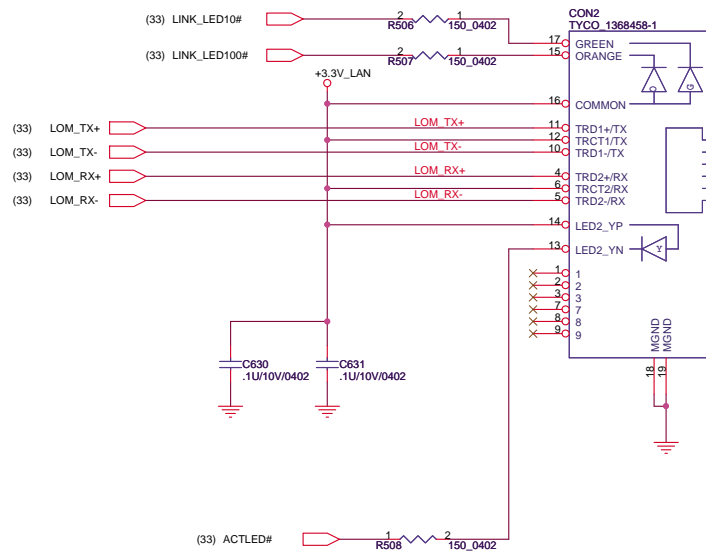
Delete R630&R631  
per 4401 ref  
schematic

C624  
1U/10V/0402

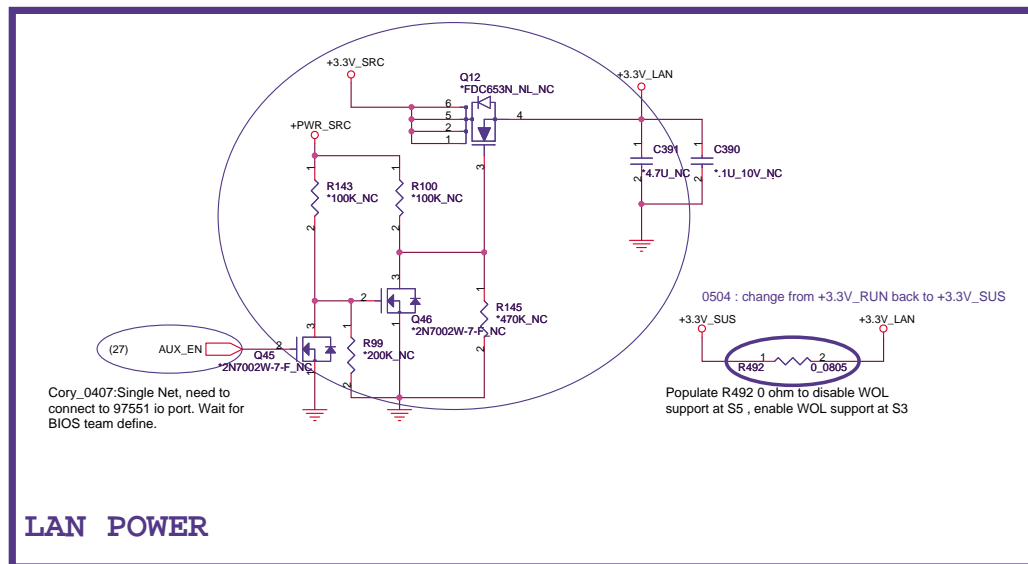
C625  
1U/10V/0402

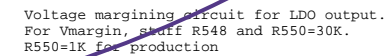
**Note:** The BCM4401 has weak internal pulldown resistors on the following signals:  
SPROM\_CS, SPROM\_CLK, SPROM\_DOUT, SPROM\_DIN.

Title				LAN(BCM4401)			
Size		Document Number FX2					Rev 1A
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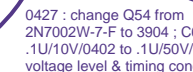
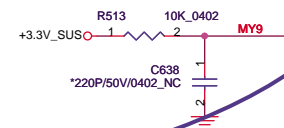


- change name for ED5
- copy ED5 to FX2
- Waiting to check
- copy DM5 to FX2

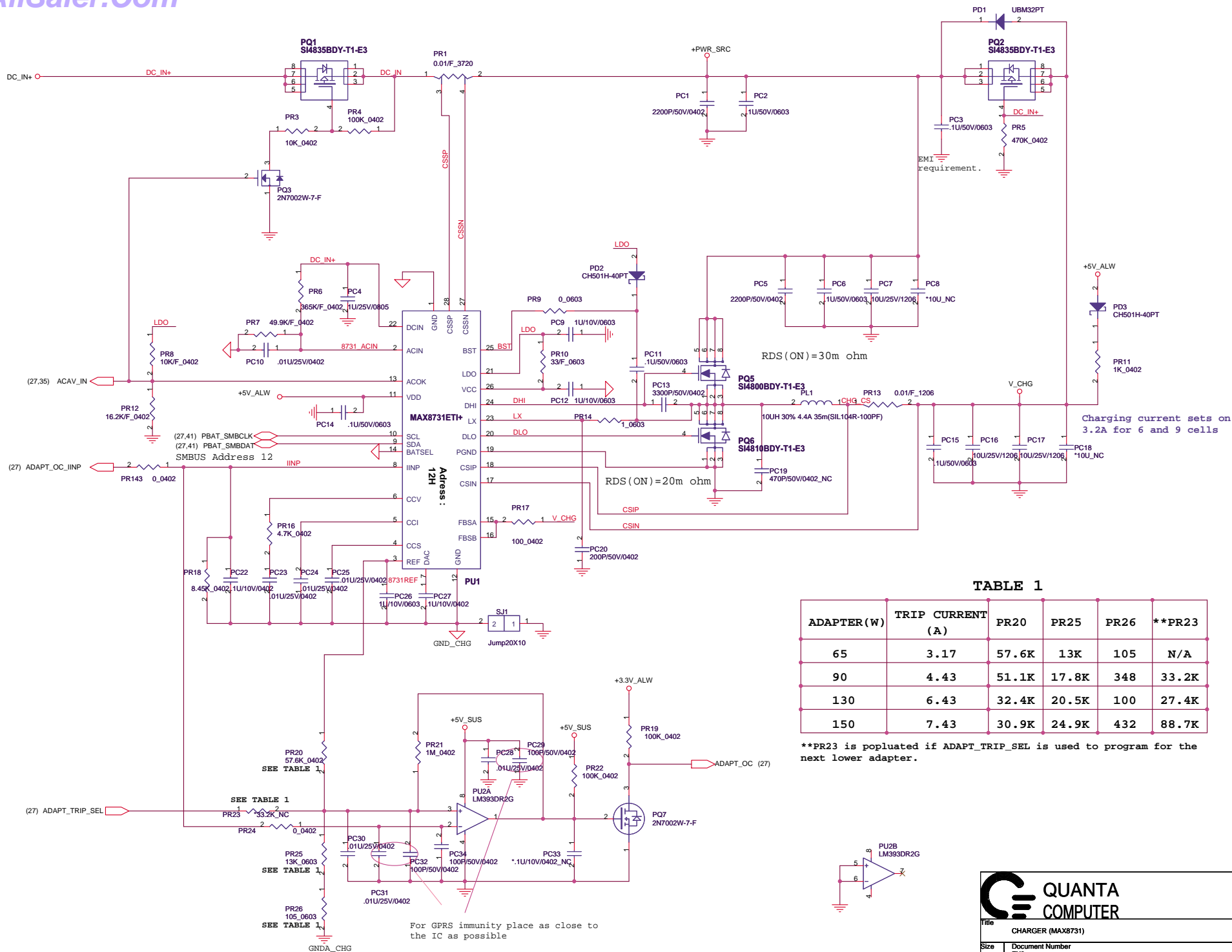




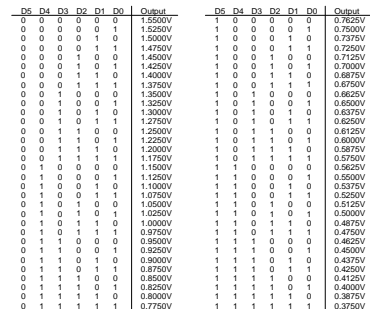
as FM1 keyboard matrix & "e0788.1104a\_swap-0422"

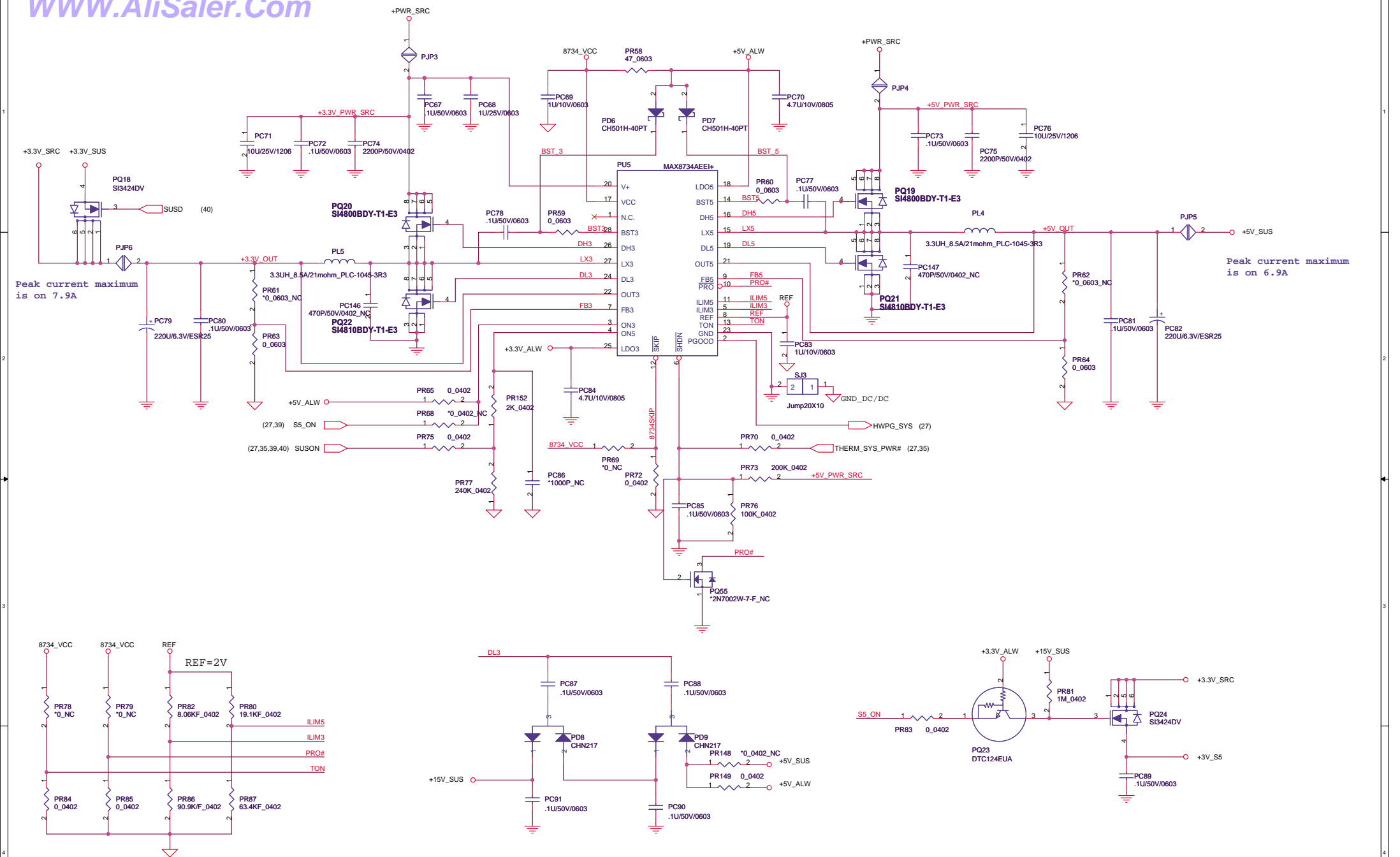


**KBC**

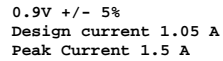
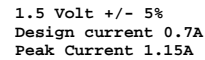




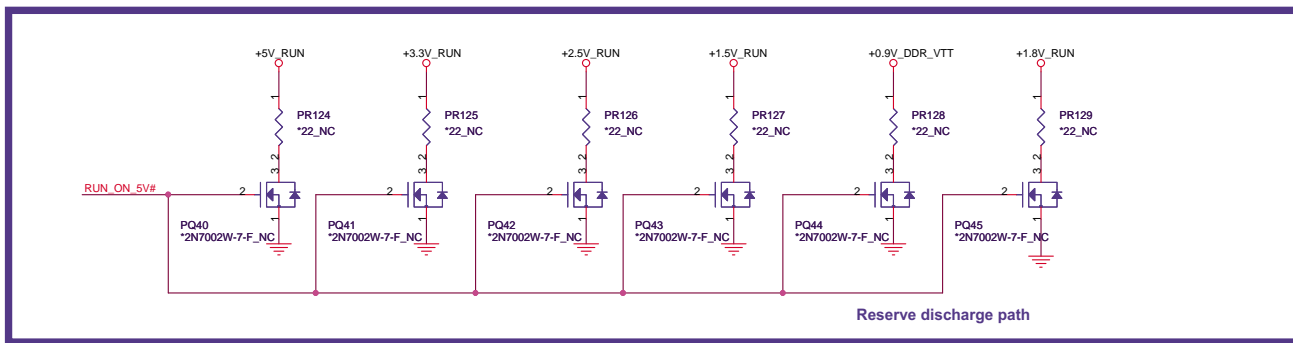
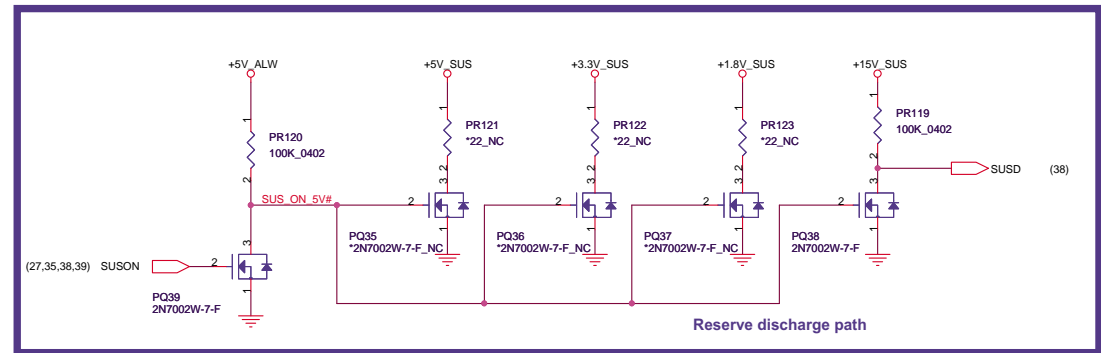
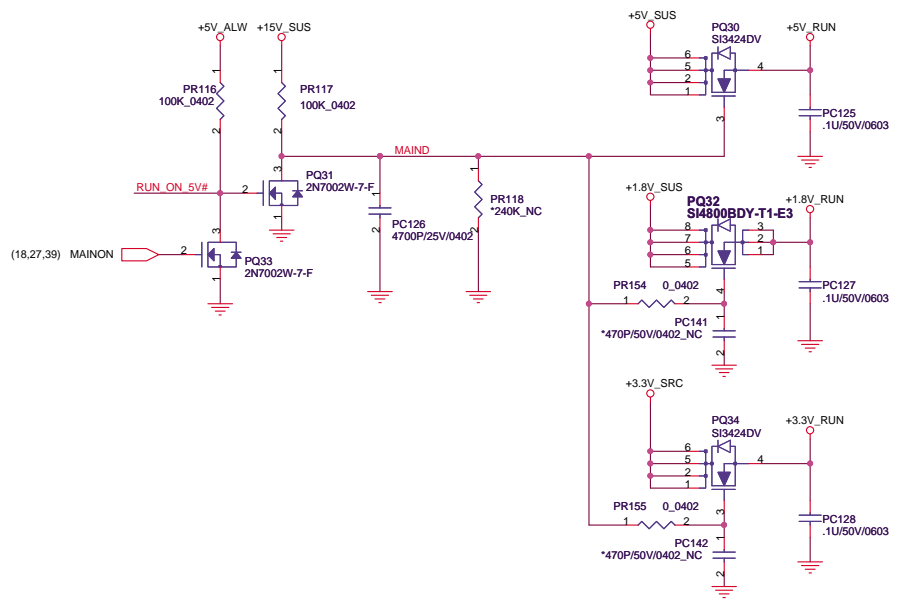





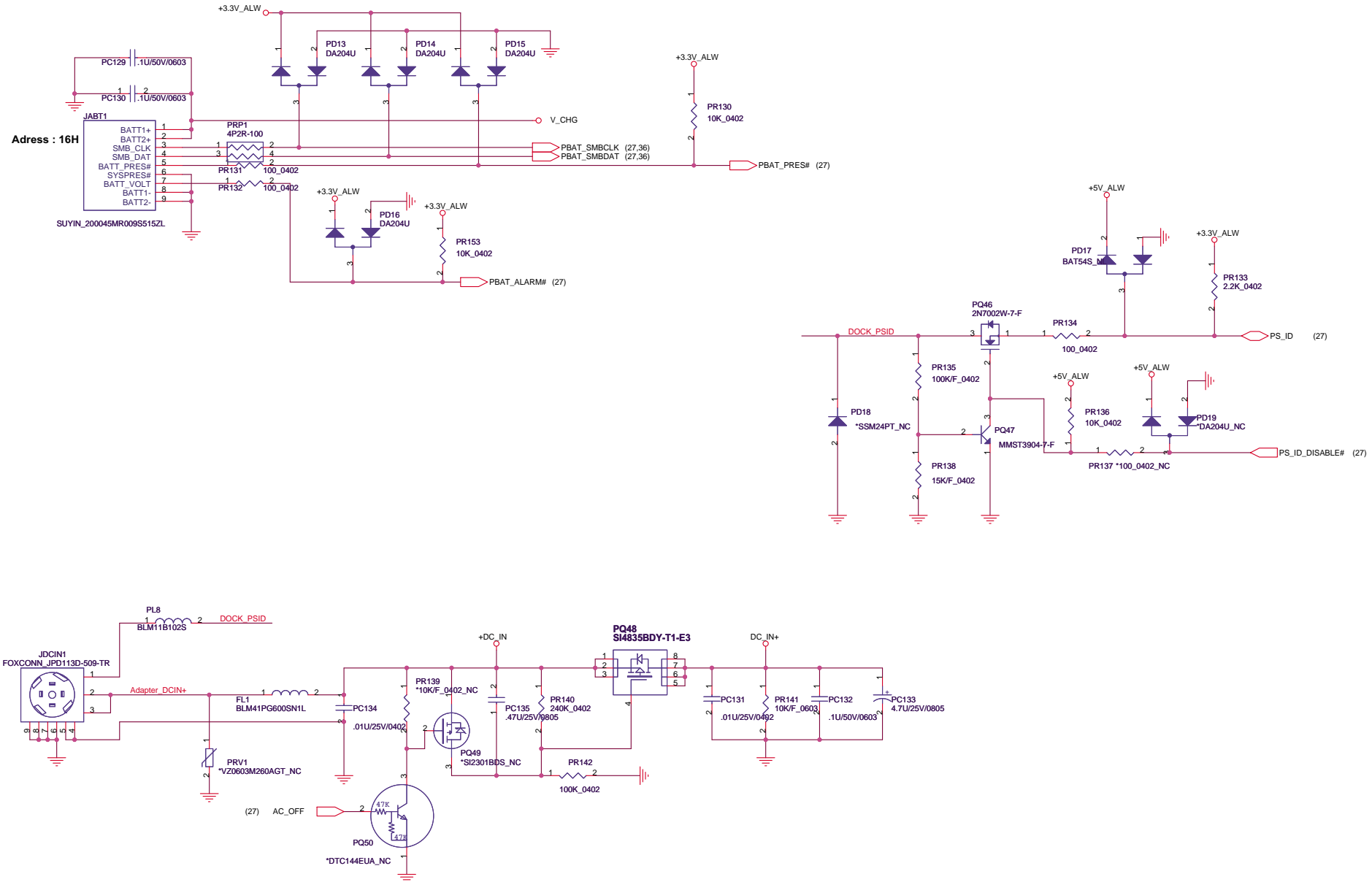
Title			SYSTEM (MAX8734)
Size	Document Number	Rev	1A
FX2			
Date:	Friday, May 05, 2006	Sheet	38 of 47




Title			
VCCP			
Size	Document Number	Rev	
	FX2	1A	
Date:	2005/4/21	Sheet	39 of 47



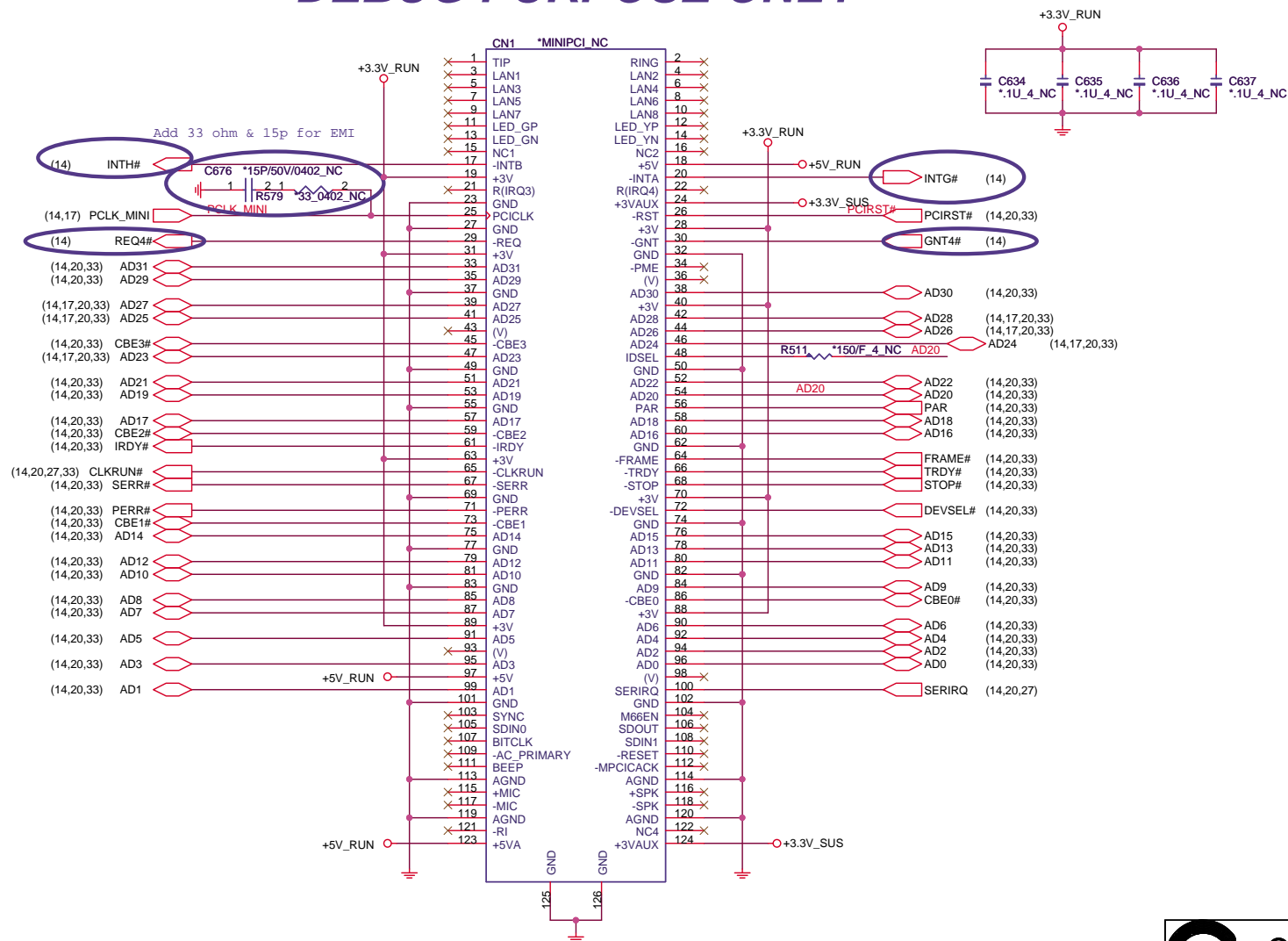
 <b>QUANTA COMPUTER</b>		
Title RUN POWER SW		
Size	Document Number FX2	Rev 1A
Date:	Friday, May 05, 2006	Sheet 40 of 47



 <b>QUANTA COMPUTER</b>		
Title	DCIN,Batt	
Size	Document Number FX2	Rev 1A
Date:	Friday, May 05, 2006	Sheet 41 of 47

ID Select : AD20  
Interrupt Pin : INTG# , INTH#  
Request Indicate : REQ4#  
Grant Indicate : GNT4#

# DEBUG PURPOSE ONLY

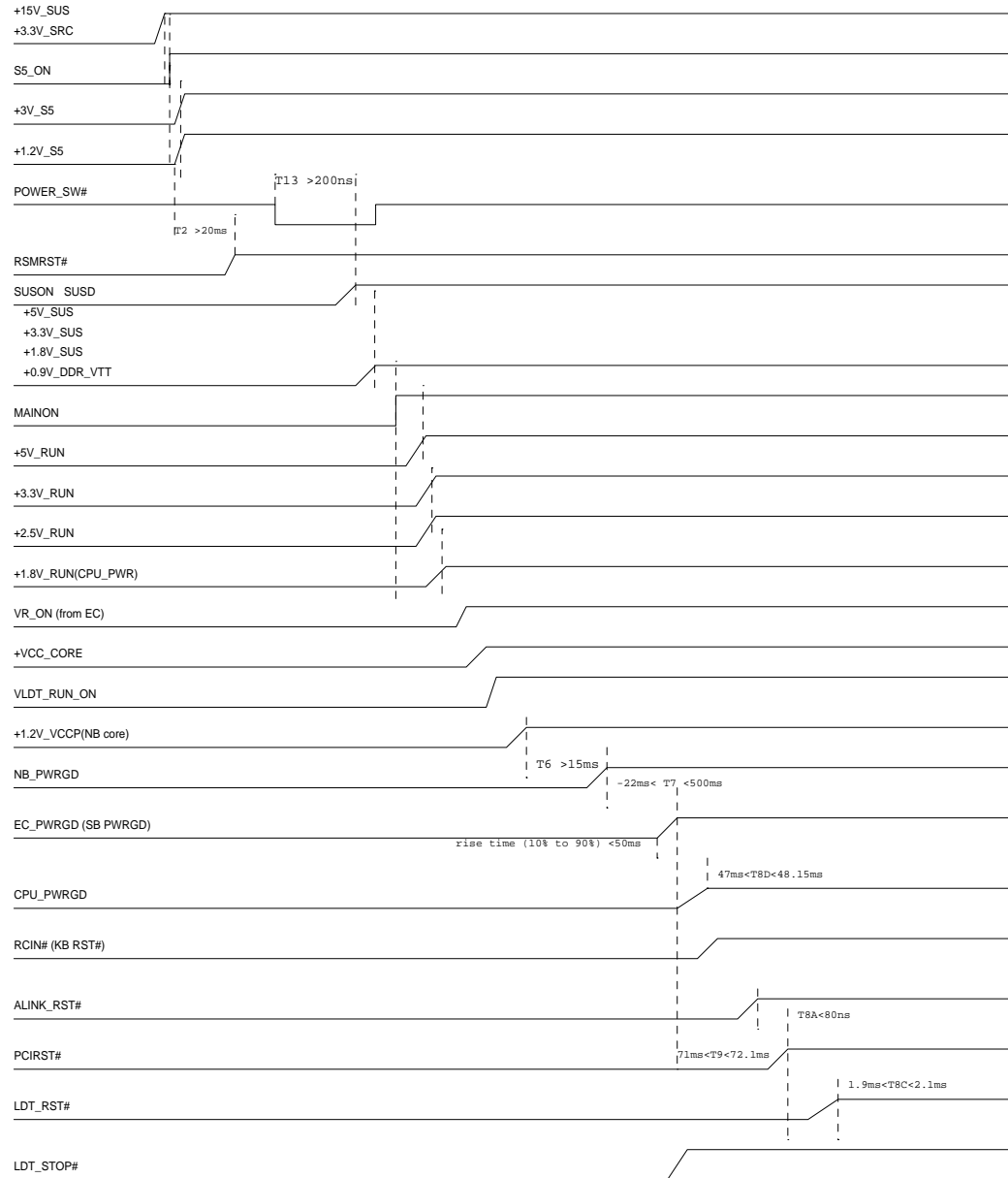


MPC



Title		
MINI PCI(for debug)		
Size	Document Number	Rev
FX2		1A
Date:	Friday, May 05, 2006	Sheet 42 of 47

## Power On Sequence

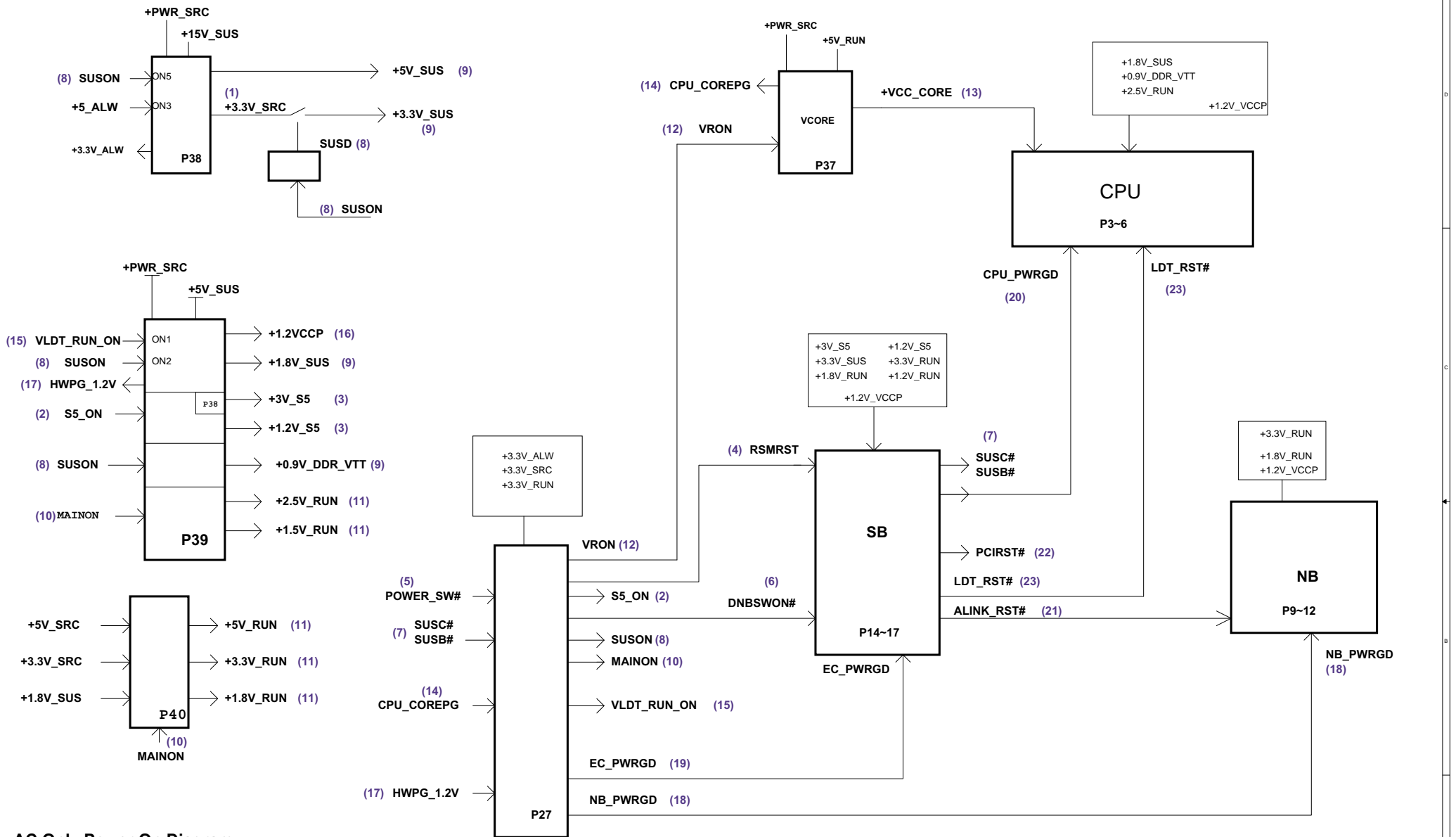


T6: NB core voltage to NB\_PWRGD  
T7: NB\_PWRGD to SB\_PWRGD  
T8D: SB\_PWRGD to CPU\_PWRGD

T8A: ALINK\_RST# to PCIRST#  
T9: SB\_PWRGD to PCIRST#  
T8C: PCIRST# to LDT\_RST#

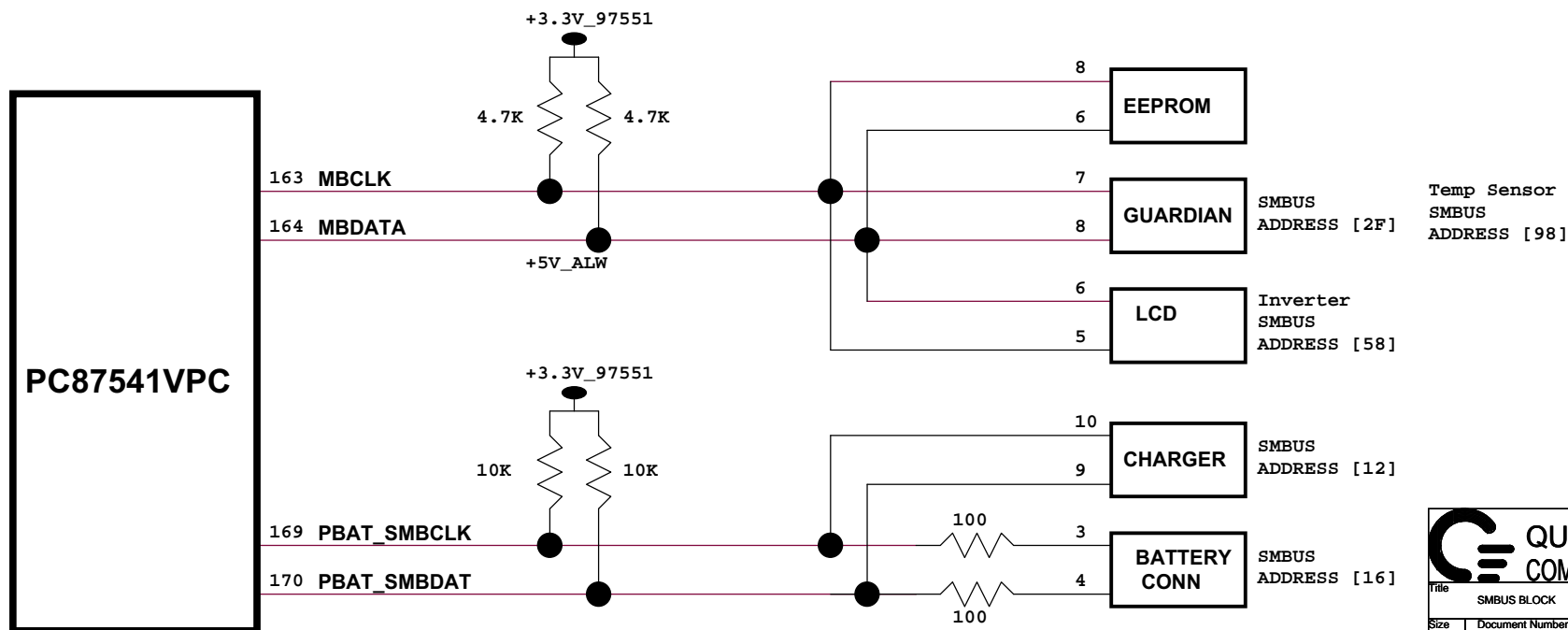
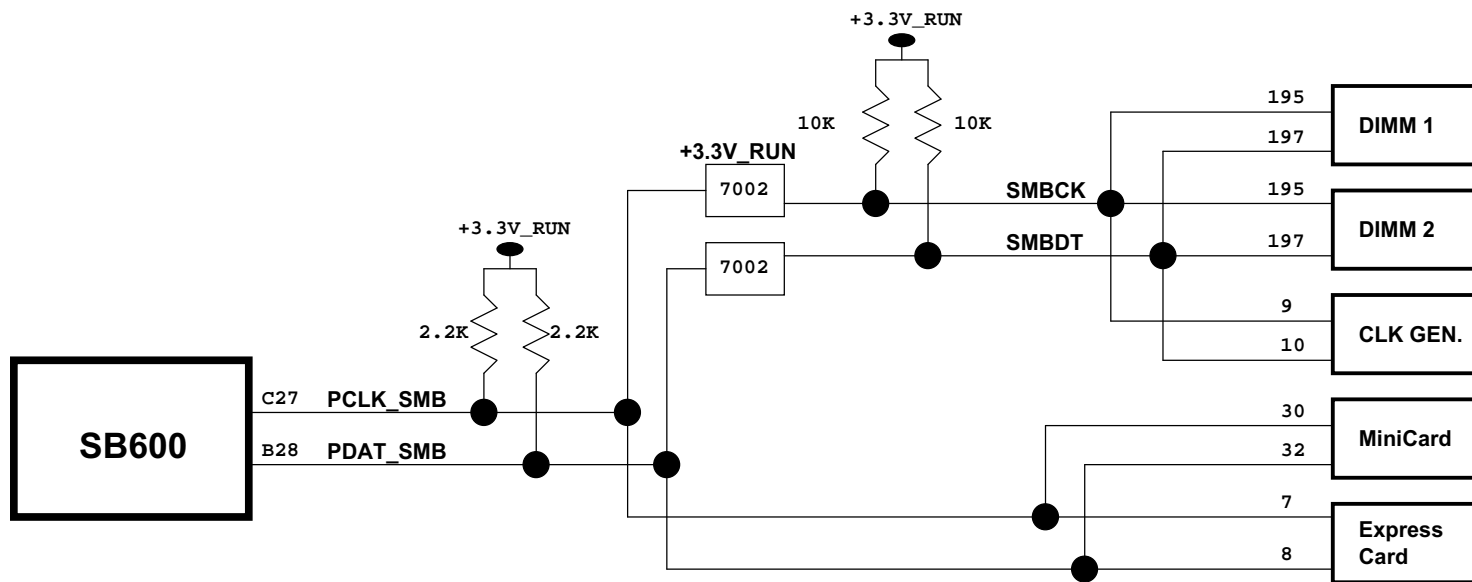
<b>QUANTA COMPUTER</b>	
Title: Power On Sequence	
Size: FX2	Document Number: FX2
Date: Wednesday, May 10, 2006	Sheet: 43 of 47
Rev: 1A	





AC Only Power On Diagram

- |                      |                         |                  |                 |
|----------------------|-------------------------|------------------|-----------------|
| (1) +3.3V_SRC        | (8) SUSON, SUSD         | (13) +VCC_CORE   | (20) CPU_PWRGD  |
| (2) S5_ON            | (9) +5V_SUS             | (14) CPU_COREPG  | (21) ALINK_RST# |
| (3) +3V_S5, +1.2V_S5 | (10) MAINON             | (15) VLDT_RUN_ON | (22) PCI_RST#   |
| (4) RSMRST           | (11) +5V_RUN, +3.3V_RUN | (16) +1.2_VCCP   | (23) LDT_RST#   |
| (5) POWER_SW#        | (12) VRON               | (17) HWPG_1.2V   |                 |
| (6) DNBSWON#         |                         | (18) NB_PWRGD    |                 |
| (7) SUSC#, SUSB#     |                         | (19) EC_PWRGD    |                 |



<b>QUANTA COMPUTER</b>		
Title: SMBUS BLOCK		
Size: FX2	Document Number: 1A	Rev: 1A
Date: Friday, May 05, 2006	Sheet: 45	of 47